Defect-Based Testing of LTS Digital Circuits

Arun Antony Joseph

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OF
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Born on 31st May 1978
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I am the Lord, and there is no other; There is no God besides Me. I will gird you, though you have not known Me, That they may know from the rising of the sun to its setting That there is none besides Me. I am the Lord, and there is no other (Is 45: 5 – 6)

The fool has said in his heart, "There is no God." (Ps 14:1; Ps 53:1)

- The Bible

To my God & Savior Lord Jesus Christ

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Chapter 1

Introduction

Many of the semiconductor technologies are already facing limitations while new-generation data and telecommunication systems are implemented. Although in its infancy, superconductor electronics (SCE) is capable of handling some of these high-end tasks. Test methodologies for SCE are yet to be developed. A defect-based test methodology for SCE is presented in this thesis, so that systematic testing of complex systems can be implemented in this technology. In this chapter, the applicability of SCE is presented. The major issues to be tackled with regard to SCE and the outline of the thesis are also described in this chapter.

1.1 Emerging High-Speed Applications

Requirements for efficient new-generation electronic systems in data and telecommunication industries are pushing the semiconductor technologies to their limits. Applications such as Software-Defined Radio (SDR) [1], petaflop computers [2] and high-speed network routers [3] are extremely difficult to implement and are very complex in nature. As the RF and digital domains converge, entirely new strategies are needed to enable the innovative applications that will drive tomorrow's electronics industry.

The wireless communications industry with its unquenchable thirst for bandwidth in digital telecommunications requires future data converters and digital signal processors to deliver greatly increased performance to meet the connectivity demands of users. Due to the rapid increase of mobile communication systems, the available RF spectrum gets more and more crowded. Hence an efficient frequency allocation and usage is necessary to meet the demands of industry. SDR for Base Station (BS) applications, where analog-to-digital conversion is one of the enabling technologies, as explained in [1], is a promising concept for the wireless communication industry since the entire transceiver function can be implemented in software, avoiding the replacement of hardware each time the system has to be upgraded.

However, the practical implementation of such a system is dependent on the hardware, which consists of precise, ultra high-speed electronic devices such as Analogue-to-Digital Converters (ADCs). The present and near future semiconductor ADCs cannot be used for the implementation of SDR BS in the near future [4]. Some of the factors that hamper the implementation are the requirements of very high speed at a few tens of GHz and the high resolution (e.g. 16 bits) at these speeds and bandwidth.

The hyper-computer business demand for access to intensive computation for weather prediction, non-invasive geo-physical exploration of natural resources, global economic modelling, intensive data mining, and other applications already exceeds the abilities of modern supercomputers and networks. Ever-faster processing capabilities, ultra-low latency memories, and ultra-high throughput network switches will be required in the future.

Currently, high-performance CMOS-based microprocessors have reached a clock frequency of about 4 GHz, and a microprocessor assembly featuring about 125 million transistors are placed on a single 112 mm^2 chip [5]. The heat dissipation in the worst case situation can be up to about 115 watts (similar microprocessor for mobile applications can dissipate up to 88 W at 3.5 GHz while those for embedded applications up to 27 W at 2 GHz) [6]. The peak performance of such a CMOS multiprocessor chip can be crudely estimated as 10 to 100 gigaflops based on a very optimistic assumption of the fabrication technology [7].

To achieve a peak performance of 1 petaflops will take 10 to 100 thousand advanced CMOS chips discussed above, with total power consumption in the order of 10 MW. The management of power of such proportions would take a sizeable building. The significant (microsecond-scale) latency of interprocessor communication in a system of such a

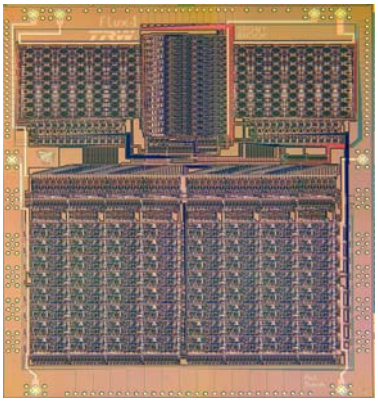

Figure 1.1: Microphotograph of the Flux-1 RSFQ microprocessor (Courtesy: NGST).

physical size would make the system stall for programs where inter-processor communication is a significant fraction of the computational process. More recent semiconductor technologies like the complementary GaAs technology are also far behind in performance for these requirements [8]. Alternatives like grid computing using distributed computing principles are being tried extensively to solve the need for high-performance systems [9].

Furthermore, the defense/government market with a never-ending drive to do more with less is resulting in a concentrated push to deploy multifunction, dynamically reconfigurable systems. Such systems will rely on flexible, ultra-fast, digital technologies, and replace, consolidate, and expand the capability of existing dedicated analogue systems for radar, electronic warfare, and other surveillance applications.

1.2 Super-Conductor Electronics (SCE)

In the near future, current semiconductor technologies will not always be able to provide efficient solutions for the speed, accuracy and power requirements for the applications mentioned in the previous section. SCE is an emerging technology in which the active element, a Josephson Junction (JJ), work in the superconducting state of the materials used for its fabrication. The operating temperatures of these systems are much below room temperature. According to the International Technology Roadmap for Semiconductors (ITRS) 2005, SCE will address several important specific applications that are beyond the scope of semiconductors [10]. A detailed discussion about SCE is presented in chapter 2 of this thesis.

A number of commercial enterprises have started developing systems in SCE. IBM was one of the first to start research in SCE. But the activities were stopped due to problems in the pre-mature technology for realizing these SCE circuits. Later, after the invention of Rapid Single-Flux Quantum (RSFQ) logic [11], and the development of the planar tri-layer process [12], the limitations in realizing medium-complex SCE circuits were eliminated. In

the past few years, extensive research has been carried out with regard to the development of high-end complex systems in SCE. Examples of these complex designs are a superconductor ADC [13] targeted towards SDR BS developed by MIT in collaboration with IBM which was fabricated by HYPRES Inc. NY, the Flux microprocessor chip [14] for the US defense petaflops program by TRW Space and Electronics (now Northrop Grumman, CA) as shown in Figure 1.1 and a GHz packet switch [15] by NEC, Japan for high-speed networks.

RSFQ logic is a new family in SCE for future Integrated Circuit (IC) technology with the potential to leapfrog the performance of traditional silicon and III-V compound semiconductors. ICs with sub-micron RSFQ static digital frequency dividers and Toggle flip-flops have already been fabricated and operated in university laboratories at over 750 Gb/s [16], [17]. These achievements represent faster demonstrated electronic circuit speeds than any other technology has predicted today, even via computer simulations.

The RSFQ technology also has a clear path to extend performance. Unlike semiconductor devices, the speed of RSFQ ICs comes from inherent physical phenomena, not advanced scaling. This means that existing lithography techniques can be employed, and more importantly, existing equipment can fabricate circuitry that surpasses conventional limits of performance. Because RSFQ logic uses the lossless ballistic transmission of digital data as “fluxons” or a magnetic-flux quantum near the speed of light, the wire-up nightmare that silicon designers face is substantially reduced. This scenario also allows the full speed potential of individual gates to be realized.

The speed and power problems associated with semiconductor processors have stimulated a search for alternative approaches to petaflops-scale computing. Preliminary design work shows that an RSFQ microprocessor using a much more conservative, 0.3 μm fabrication technology can house just about 30 million JJs (active elements) on a chip of comparable area. Operating at a clock frequency of about 90 GHz it would be able to provide a peak performance of approximately 2,000 gigaflops, while the dissipating power would be below the 1 Watt level. The Hybrid Technology MultiThreaded architecture (HTMT) project based on the use of RSFQ technology with its “COOL” core [7] indicates that the 1-petaflops peak performance might be reached with just 500 logic chips (plus about 2,000 fast superconductor memory chips), with aggregate power dissipation in the core below 1 kW. Although the removal of such power from the cryostat (the container in which the RSFQ IC chips are kept at their cold superconducting temperature) would require a large-scale close-cycle cryocooler (helium recondenser) consuming about 300 kW, this is still considerably less than what would be required for a CMOS-based system. Even more important, the cryocooler would be remotely placed, enabling to compact the RSFQ core into a 1 m^3 volume. As a result, the simulated average latency of the inter-processor communication network (including both switching delays and signal time-of-flight) is as low as 20 ns, apparently enabling the system as a whole to sustain a sub-petaflops performance in many real-life computer programs [18].

Other features of this technology that make it suitable for growth into the traditional market include its compatibility with existing IC packaging techniques. These include

compatibility with optical (fiber) signal input and output, a maturing multi-chip module (MCM) technology with multi-Gb/s digital data transfer between chips, and simple interface circuits to convert to and from both ECL logic and CMOS logic levels [19], [20].

Even at this immature stage, SCE is capable of handling these tasks. Having a very high theoretical speed limit with the accuracy of a magnetic-flux quantum and very-low power consumption, SCE is a promising candidate for the high-end future applications. The most important hallmarks of SCE are summarized as:

• extremely non-linear current–voltage (I–V) and resistance–temperature (R–T) characteristics of the active elements, the JJs;

• high frequency of operation;

• high resolution and speed;

• magnetic-flux quantum limited sensitivity;

• low dissipation, dispersion, noise and loss;

On the other hand, there are reasons and situations, which may decrease the motivation for using SCE:

• cooling and cryogenics add additional costs, power requirements, weight and possible vibrations to the system;

• its sensitivity could in some cases mean saturation from other incoming signals or from electromagnetic interference (EMI) and hence special care has to be taken;

• if price versus performance gives no advantage (for e.g. small scale applications);

• if other technologies solve the problem more efficiently (for e.g. usage of SCE in a personal computer).

Main disadvantage of an SCE system is the requirement of cooling the device to superconducting temperatures. But the high-end applications such as SDR and petaflops computer require cooling even if semiconductor technologies are used and intense research is carried out to bring the SCE systems like an ADC to “high” temperatures by developing them in high-temperature superconductor (HTS) technology as opposed to low-temperature superconductor (LTS) technology. SCE finds its application when ultra-high speed switching or processing of large volume of data per unit time is required.

1.3 Problem Definition and Chosen Approach

Since RSFQ circuits work at extremely high speeds, testing and verification of such a device is a difficult and challenging task. Direct testing at these speeds is not possible at this moment. Furthermore, the costs of the equipment required for such tests would be extremely high. Hence methods have to be developed to reduce the requirements of external hardware for the test. In systems consisting of several thousands of gates, the trend

is to introduce certain testability options at the design phase. Main goal of this Design for Testability (DfT) approach is to enable structural testing and Automatic Test Pattern Generation (ATPG) by insertion of additional logic. This is desirable, as the system under study is complex; hence it is not possible to test all components directly within the system. A DfT-based approach is essential for commercial production of complex systems in SCE.

As the complexity of the SCE circuits has increased beyond 63,000 JJs per chip as in the case of a Flux microprocessor chip [14], realization of a working design becomes an extremely difficult task. Although extended research is going on in making complex circuits and scaling down the minimum sizes, very little or no information is available in the literature on the methodology for defect analysis for superconductor electronics. The yield levels are much lower in SCE than in the semiconductor industry. One of the reasons is due to the fact that little information is available on superconductor process defects and hence little improvement can be made.

In semiconductor microelectronics, special test structures have been developed and realized along with the functional integrated circuits. The information gathered using these test structures are used for yield analysis and improvement and defect-oriented testing. As mentioned before, little information is available on probable defects in SCE process and test methodologies. More detailed information supporting this issue can be found in the special issue on applications of superconductivity of the Proceedings of the IEEE [21].

Development of a measurement methodology for defect analysis in SCE was one of the problems that have been tackled during our research. Major issues handled during this process were ease of measurement and measurement time for quick determination of the existence of defects. For this purpose, two RSFQ processes were investigated and subsequent results are presented in this thesis [22]. Special test structures were developed and realized along with the ICs for the RSFQ process. The measurement methodology and results on structures that have been developed to detect the top-ranking defects that can occur in a Niobium tri-layer based technology are presented [23].

The information gathered using these test structures are primarily used for DBT. Based on this information, a DBT has also been conducted and those results are presented leading to possible test methodologies for RSFQ circuits. From the data, potential defect-prone areas can be detected within the circuit and DfT structures can be introduced to monitor the status while employing the DBT approach. In this thesis, the possibilities of DfT for SCE circuits in view of the DBT approach are also presented.

Fault models have been developed after studying the behaviour of the test structures. These fault models are subsequently used for fault simulation of the circuit for development of an ATPG technique. The ultimate goal is to develop ATPG for SCE logic circuits. Investigating the possibility of whether or not the available ATPG techniques are applicable is one of the major concerns in the process. Otherwise new ATPG techniques have to be specifically developed for SCE. Information about defects and their subsequent translation into fault-models are crucial at this stage as little is known about the defects that

can occur in an SCE fabrication process [21], and especially under superconducting circumstances.

As part of DBT, various fault models have been proposed for SCE circuits. These are theoretical models based on work in structural testing and analysis of SCE processes. Until now, such models have not yet been verified. As the ultimate goal is to develop ATPG for SCE circuits to guarantee a high quality, verified fault models are required before going ahead with ATPG approaches. A test methodology based on a DfT approach is required for the physical verification of the abstracted fault models. The fact that an individual Single Flux Quantum (SFQ) pulse is extremely difficult to be detected was hampering the verification process. DfT schemes have been proposed to detect an individual SFQ pulse [24]. This technique is applied to a simple RSFQ logic circuit to verify the proposed fault models.

As a continuation of the research in DBT of an RSFQ D-type Flip-Flop (DFF), extensive studies were conducted on such a DFF realised in a mature Nb process at HYPRES Inc., NY. HYPRES is one of the leading SCE foundries where commercial production of RSFQ devices has been started. The defect-prone locations in the DFF were identified and defects were deliberately inserted into the device. Simulation experiments showed that ATPG could be possible with adaptation/modification of the techniques for SCE, but needs verification by means of extensive experiments. Ultimately, the development of SCE systems including DfT hardware is required if they are to be used in commercial applications [25]. In our investigation, Built-In-Self-Test (BIST) feasibility study was carried out for an SCE Delta ADC being developed for SDR application. But the focus changed to defect detection and fault models as the relevant metrics were not available to proceed with BIST [26].

1.4 Outline of the Thesis

In this section, the outline structure of the thesis will be discussed.

Chapter 2 introduces the reader to the RSFQ logic family of circuits. The chapter starts with an introduction to SCE. A JJ is described along with circuit models and associated SCE circuits in the RSFQ logic family are presented in detail. The design and implementation of RSFQ circuit with an example of a DFF is also elaborated. Advantages and disadvantages of using RSFQ circuits based on the latest developments are in addition mentioned in this chapter.

Chapter 3 starts with an introduction to IC testing. Functional, structural and DBT is elaborated followed by the selection of defect-monitor test structures for fabrication process analysis. Various types of structures are mentioned and the measurement techniques used for them is explained. DfT is discussed with possible structures for the defect-based testing of RSFQ circuits. It is demonstrated how SFQ pulses can be monitored at an internal node of an SCE circuit by Test Point Insertion (TPI). The available features in the proposed design for customising the detector make it attractive for a detailed DBT of

RSFQ circuits. The introduction of a test signal in an RSFQ circuit using TPI is also being illustrated.

Chapter 4 starts with a short introduction of superconductor processes used for RSFQ circuit realisation. Different types of processes are mentioned to get a general idea about them. Finally, the two LTS RSFQ processes which were investigated during this research work are presented in detail. A structural measurement methodology has been applied to both processes, leading to the detection of various probable defects that can occur in them. Defect-monitor test structures were developed as part of the research so as to determine the defect statistics in these processes. The applied test methodology as well as the structures are presented in detail for both processes. This chapter concludes with the design implementation of test chips incorporating the above mentioned test structures. The classification of defects in an RSFQ process is also presented.

Chapter 5 deals with the experimental analysis of the test chips developed for the structural testing of RSFQ processes. The two processes described in the previous chapter which were investigated during this research work are analysed. Methodologies for the measurements are also presented. Implementation of the test-routines for semi-automatic testing of the processed chips for structural defects at room temperature has been carried out. The test data is analysed to provide defect statistics of both processes. This chapter presents the defect ranking of the processes leading to the most probable defects in a process. Measurement methodologies for low temperature (LT) measurements are also presented and it is proven that the approach is able to detect the defects in a JJ. A DBT approach is presented for fabrication-process analysis. The presented defect-monitor structures are used to gather statistical information, i.e. the probability of the occurrence of defects in the process. This forms the first step for Inductive Fault Analysis (IFA), a commonly used DBT methodology.

Chapter 6 deals with the methodologies applied for the testing of RSFQ circuits. Modelling and the influence of a defect that can create an error in an RSFQ circuit are subsequently described using circuit simulations in Chapter 6 of this thesis. Development of fault models for RSFQ circuit testing is covered in this chapter based on the results from the developed defect-monitoring test-structures. Two types of DBT methodology are enumerated in this chapter. The preliminary investigation leads to a detailed study on an RSFQ DFF. Test chips have been developed incorporating defect-induced DFFs to study the actual behavior when the probable defects are present in the realized circuit. This chapter concludes with the design implementation of test chips which will be used for the verification of the developed fault models in the future.

Finally, Chapter 7 gives a summary of the obtained results. The conclusions are discussed with future research possibilities into ATPG and yield analysis of RSFQ-based systems.

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Chapter 2

Superconductor Electronics for Digital Applications

This chapter introduces the Rapid Single Flux Quantum (RSFQ) logic family of circuits. It starts with an introduction to Super-Conductor Electronics (SCE). A Josephson junction (active element) is described along with circuit models and associated SCE circuits and the RSFQ logic family is presented in detail. The design and implementation of RSFQ circuits with as example a D-type flip-flop is also discussed. Advantages and disadvantages of using RSFQ circuits and the latest developments are also mentioned in this chapter.

2.1 Introduction

As mentioned in the previous chapter, Superconductor Electronics (SCE) is emerging as one of the technologies for future high-end applications. Various schemes were proposed for implementing logic circuits in SCE. Now-a-days, the most widely used SCE logic is Rapid Single Flux Quantum (RSFQ) logic and the essential elements are Josephson Junctions (JJ), inductors and resistors for biasing and shunting the junctions. A JJ, the basic active element of an SCE circuit, is formed if two superconductors are separated by an interface of nanometre dimensions. The operation of a JJ is based on the quantum mechanical tunnelling across this dielectric barrier interface [1]. Inductors are of two types, storage and normal (non-storage). Storage inductances have relatively higher values than normal ones, so that the loop containing a JJ will be able to store a magnetic flux quantum or a fluxon [2]. RSFQ circuits use very little power because they remain in superconducting state except while switching of a JJ during its operation, which lasts only for a few pico-seconds. In practice, a negative bias voltage, resulting in a negative bias current, is applied to the RSFQ circuit for the correct operation.

The Josephson Effect was predicted by Brian Josephson in 1962 while he was a student at Cambridge University [3]. The first Josephson devices were made by Philip Anderson and John M. Rowell at Bell Laboratories in 1963 [4]. In a modern Josephson device, the operation is resulting from the tunnelling of electrons pairs through its thin barrier. These pairs of electrons, called Cooper pairs, carry current in superconductors [5]. The insulating barriers are called weak links because the Cooper current through them is only a small fraction (~ 1/1000) of the maximum pair current that can be carried in the superconductor electrodes. Tunnelling through the gate oxide is undesirable in silicon field effect transistors, while in Josephson junctions the tunnelling current is essential. From the mid-’60s to the mid-’80s, superconductor digital ICs relied on logic schemes in which Josephson junctions with hysteretic I-V curves were switched from the superconducting (0) state to the resistive (1) state. In today’s RSFQ technology, the junctions are shunted externally with a resistor, so the I-V characteristic becomes nonhysteretic. This allows circuit designers to exploit another superconductivity phenomenon: the macroscopic quantization of magnetic flux [1]. In RSFQ circuits, it is not a static voltage level, but the presence or absence of quantized magnetic flux or fluxons that represent information bits [6], [7].

The organisation of the chapter will now be outlined. Section 2.2 deals with a JJ and associated models. JJ circuits are described in Section 2.3. Design and implementation of RSFQ circuits are presented in Section 2.4. Advantages and disadvantages of RSFQ circuits are described in Section 2.5.

2.2 Josephson Junctions

The fact that a superconductor can exist in two states: the resistive (normal) state and the superconducting state, is used for practical applications involving switching. One of the first devices to be used in logic operations was a cryotron [8] proposed by Dudley Buck of

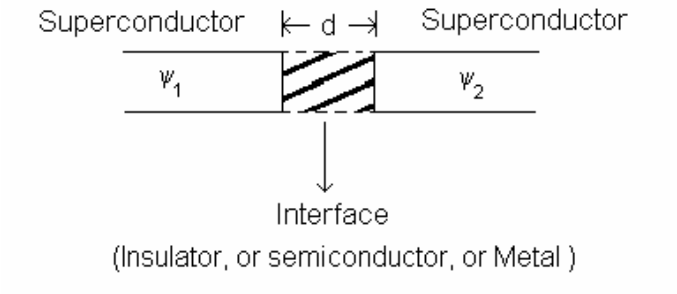

Figure 2.1: Schematic of a Josephson junction.

MIT Lincoln Labs in 1956 and was the first practical application of superconductivity. It consisted of a short gate wire of a low critical-field superconductor surrounded by a solenoid coil of a high critical-field superconductor. A sufficient solenoid current I_c can cause the field at the surface of the gate wire to exceed the critical current, therefore causing the gate wire to exceed the critical field and causing the gate to become resistive. If I_c is then reduced, the gate again becomes superconductive. Several circuits were suggested using a cryotron, a detailed discussion can be found in [9]. The major problems faced were reproducibility and yield. The basic devices were predicted to have an operating frequency of up to a few hundred MHz. Another factor which had to be taken care of was avoidance of high-inductance loops as well as a high relative power consumption.

As mentioned before, the discovery of the Josephson Effect made a difference in SCE. A JJ is formed if two superconductors are separated by an interface which can be an insulator, metal or semiconductor with a thickness of a few nanometres. Figure 2.1 shows a schematic of a JJ. If ψ_1 and ψ_2 are the macroscopic wave functions describing the superconductors with a phase difference of ϕ, a supercurrent will flow through the JJ [1]. This supercurrent is not a function of voltage, but of the phase difference of the wave function between the electrodes and is given by the equation:

$$I_s = I_c \cdot \sin \phi \tag{2.1}$$

where I_c is the critical current being the maximum supercurrent that the junction can handle. This is called the DC Josephson effect: a supercurrent can flow through a JJ, without a voltage being present across the junction. This holds for supercurrents smaller than the critical current of the junction. The presented situation is referred to as the superconducting or stationary or S-state of the junction. If a voltage V is applied across the JJ, the phase difference ($\phi = |\psi_1 - \psi_2|$) will vary and the current across the JJ will oscillate with frequency:

$$\omega = \frac{2e}{\hbar} \cdot V \tag{2.2}$$

and amplitude I_c, where e is the elementary charge ($e \approx 1.60 \cdot 10^{-19}$ C) and ħ is given by:

$$\hbar = \frac{h}{2\pi} \tag{2.3}$$

where h is the Planck's constant ($h \approx 6.63 \cdot 10^{-34}$ Js). This is called the AC Josephson effect and given by the equation [10]:

$$\omega = \frac{d\phi}{dt} = \frac{2e}{\hbar} \cdot V = \frac{2\pi}{\Phi_0} \cdot V \tag{2.4}$$

where Φ_0 is the magnetic flux quantum; ($\Phi_0 \approx 2.07 \cdot 10^{-15}$ Vs).

If a non-zero voltage is present across the junction at a non-zero (0 Kelvin) temperature T, there will be an oscillating supercurrent I_S as well as a normal current I_N present. The normal current is due to thermal motion of the charge carriers; some Cooper pairs will be broken, after which one of the carriers will tunnel across the barrier. This current becomes dominant in the situation where the energy supplied by the voltage across the junction is greater than the binding energy of a Cooper pair (2Δ). The described situation occurs as the junction voltage approaches the gap-voltage, V_g:

$$V_g = \frac{2\Delta(T)}{e}. \tag{2.5}$$

For situations where $|V| > V_g$, the I_N-V relation can be approximated by the usual Ohmic dependence:

$$I_N = G_N V = \frac{V}{R_N} \tag{2.6}$$

where I_N is the normal current through the junction, V is the voltage over the junction, G_N is the junction's normal-state conductance and R_N the normal-state resistance. A JJ remains in its superconducting state only if the supercurrent $|I_S|$ is smaller than the critical current of the junction. Any additional current through the junction will be carried by I_N, which will result in a non-zero voltage across the junction. Therefore, when the junction current exceeds its critical current, the junction will go into the resistive or R-state.

Junctions are often characterized by their V_C parameter or "the $I_C R_N$ product". In the R-state, the supercurrent I_S oscillates with a mean value zero. When considering the I-V curve of a JJ, the oscillating supercurrent does not contribute to the DC current value. For $|V| > V_g$ the I-V relation of the junction is approximately given by equation (2.5). In case $|V| < V_g$ the mechanism responsible for the normal (tunnelling) current will not contribute. In this voltage range the DC current will consist only of the supercurrent, which has a zero mean value. A more detailed treatment on JJs can be found in [1], [10].

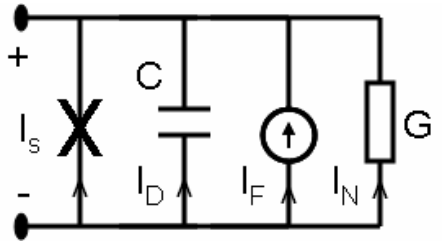

Figure 2.2: Circuit model of a Josephson junction.

2.2.1 Junction Models

One of the most widely used simulation models for a JJ is the RSJ model [11], [12] as shown in Figure 2.2. The Resistively Shunted Junction or RSJ model uses simple relationships to express the current components of a JJ. For the supercurrent it uses (2.1) and (2.4), for the normal current it uses equation (2.6). In this model two more currents occur in the junction apart from the supercurrent I_S (denoted by "X" in the model) and the normal current I_N being a fluctuation current and displacement current. The fluctuation current (I_F) is a noise current, which can for example be modelled as thermal noise. The displacement current (I_D) is a result of the capacitance of the junction in dynamic situations. The capacitance depends on junction type and size. Hence the total current will be given by the equation:

$$I(t) = I_S(t) + I_D(t) + I_F(t) + I_N(t). \tag{2.7}$$

Another model, the nonlinear-resistive junction (RSJN) model is similar to the RSJ model, except that the normal current component is approximated by the following piecewise-linear expression:

$$I_N = \begin{cases} G_L V & \text{for } |V| < V_g \\ G_N V & \text{for } |V| > V_g \end{cases} \tag{2.8}$$

where G_L is a leakage conductance that characterizes the subgap leakage current [10]. The circuit simulator used for our research was JSIM [13], a simulator developed at Berkeley University, which has been adapted for Windows at the University of Twente. The junction model used by JSIM is similar to the RSJN model. The junctions are described using the piece-wise linear curve of Figure 2.3. In this model the subgap resistance is indicated as R_0 and the normal resistance as R_N. In the JSIM model, the slope of the R-branch at the gap voltage V_g can be modelled using the *delV* parameter. The junction capacitance is not shown in the figure, but can be entered separately. Furthermore, it is possible to model the magnetic field dependence of the critical current. A more detailed treatment can be found in [1], [10], [14].

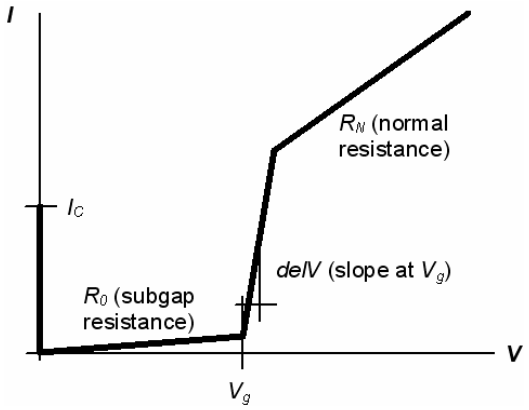

Figure 2.3: Piece-wise linear model of a JJ in the SPICE-based simulator JSIM.

2.3 Josephson Junction Circuits

The recognition of the advantages of superconductor integrated circuits has motivated several attempts to develop a practical Josephson junction digital technology, among them, the large-scale IBM supercomputer project (1969 – 1983) [15] and the MITI (Ministry of International Trade and Industry) project in Japan (1981-1990) [16] are worth mentioning. These projects were responsible for several important contributions to SCE. However, they were terminated without commercialization of the technology because the achieved circuit speed, a clock frequency of around 1 GHz in 1990, was only marginally higher than that of the fastest contemporary semiconductor transistor circuits (GaAs), and could not justify the necessary Helium cooling. The main factor limiting the speed was the unfortunate choice of the so-called latching (or "voltage-state") circuitry based on the properties of unshunted JJs as explained later. Furthermore, the Lead alloy technology used for the realisation of JJs had thermal cycling problems.

As can be shown from equations (2.4) and (2.7), such unshunted JJs, if biased with a DC current within the range $-I_C < I < +I_C$, have two different states: a superconducting state with vanishing voltage drop V across the junction, and a resistive state with $|V| \approx V_g = 2\Delta(T)/e$. In latching logic, the superconducting state is used to denote a binary “0”, while the resistive state represents binary “1”. A switching from “0” to “1” is rather fast; a few picoseconds for junctions with high critical current density, J_C of a few kA/cm^2. However, the reciprocal switching (“1”→”0”) is much more complex and is long, in the order of one nanosecond, to avoid errors. This is due to the fact that the reset cannot be achieved by merely turning the signal off as the circuit will remain in its “1” state and hence the name latching logic. The only practical way to get the state to “0” is to switch off the bias current. This is achieved by using AC rather than a DC current supply of all the gates. This is essentially the price which was paid for an attempt to mimic the information

representation by a DC voltage, which is the preferred option in semiconductor electronics, but is very unnatural for superconductors with their macroscopic quantum dynamics.

From the practical point of view, another problem of latching logic was even more drastic. Most latching devices must be driven by an external clock signal which also provides the necessary power. The total current needed to run a VLSI circuit could reach many amperes, and feeding integrated circuits with such huge currents at multi-GHz frequencies would create severe crosstalk between the off-chip segments of AC power and signal lines.

An alternative approach to use superconductors for computing is based on their natural property to quantize the magnetic flux, Φ. The flux through an element of area (A) perpendicular to the direction of magnetic field (B) is given by the product of the magnetic field density and the area elements:

$$\Phi = \int B_n \cdot dA \tag{2.9}$$

through any closed superconducting loop in multiples of the flux quantum Φ_0, ($\Phi = n \,.\, \Phi_0$). On substituting equation (2.4) written for two end points of an almost closed loop into Faraday's induction law for this loop results in:

$$\frac{d\Phi}{dt} = V \tag{2.10}$$

and integration of the resulting equation over time yields the relation between the magnetic flux and Josephson phase difference, ϕ:

$$\phi = 2\pi \frac{\Phi}{\Phi_0}. \tag{2.11}$$

Due to the relation (2.11), the variable $\Phi(r, t) = (\Phi_0/2\pi) \,.\, \phi(r, t)$ is frequently referred to as "flux" in a given point of the circuit, where $\psi(r,t) = |\psi| \exp\{i\phi(r,t)\}$ is the wave function describing the superconductor of amplitude $|\psi|$, even if it does not belong to any specific superconductor loop [2]. On a closed loop, it requires that the wavefunctions in these two (now identical) points coincide, besides there maybe a phase difference multiple of 2π. Then equation 2.11 yields the flux quantization:

$$\Phi = n \cdot \Phi_o; \qquad n = 0, \pm 1, \pm 2, \ldots \tag{2.12}$$

Recently, it was found that it is possible to fabricate and study so-called Josephson π-junctions having a ground state where the phases of the superconducting wave functions in the two electrodes differ only by π. The most interesting phenomena take place when one considers a long Josephson junction one part of which behaves as a conventional 0-junction and another part as a π-junction. There are several available technologies to fabricate such devices. At the boundary between 0 and π regions a new type of vortex (a

semifluxon) carrying only half of a flux quantum can form spontaneously. For more detailed treatment see [17], [18].

Evidently, digital information can be coded by certain values of the integer n, for example, the flux states with n = 0 and n = 1 may be used to represent binary zero and one, respectively. If a superconducting loop is made of a bulk superconductor, switching between the different flux states requires the suppression and restoration of superconductivity in at least some cross-section of the loop; the latter process would take much time, ~100 ps for Nb JJs. However, if the loop is interrupted with a JJ, switching can be performed much faster, for Nb-based junctions, actually in a fraction of a picosecond.

The basic idea of these devices is to use transient dynamics for information transfer. According to Faraday's induction law in equation (2.10), during the switching between the neighbouring flux states a short voltage pulse is formed across the junction. Since for SFQ circuits the flux change is quantised ($\Delta\Phi \approx \Phi_0$), the pulse area is also quantised:

$$\int V(t)\,dt = \Phi_0 = 2\,mV\cdot ps \tag{2.13}$$

For typical, critically shunted Josephson junctions, the FWHM (Full-Width Half-Maximum) switching time is in the order of $4\tau_0$, (i.e. a few picoseconds) where τ_0 is the transient time constant given by the expression $\tau_0 = RC = (\Phi_0 C/2\pi I_C)^{1/2}$ [2]. The amplitude of the pulse $V_{max} = \Phi_0/4\tau_0 = 1.5\ I_C R$ is in the order of a millivolt. In dynamic SFQ circuits these “SFQ pulses” are passed to other devices along either passive superconductor transmission lines or, if current/power gain is needed, active JTLs (Josephson Transmission Lines). Dynamic SFQ circuits are very attractive because the pulses can be naturally generated, reproduced/recovered, memorized and processed with simple SFQ devices whose speed is much higher and energy dissipation much smaller than that of the latching logic. Another feature which distinguishes dynamic SFQ circuits from other logic families using two-terminal devices is the pulsed nature of the signals. For such picosecond signals, even an inductance of a few pH may provide a substantial isolation between the circuit input and output. For conventional signals such as voltage steps in semiconductor electronics, three-terminal devices like transistors are very essential to provide sufficient isolation. In contrast, RSFQ circuits with their return-to-zero signals are quite robust despite using just two-terminal JJ devices, eliminating the need for superconductor transistors.

All RSFQ circuits can be divided into two groups:

a) asynchronous components with no internal memory, which generate an output SFQ pulse immediately upon the arrival of an input pulse,

b) synchronous (clocked) circuits with internal memory, where the generation of an output pulse may be delayed substantially after the arrival of data SFQ pulse(s), until the arrival of one more SFQ pulse playing the role of clock signal.

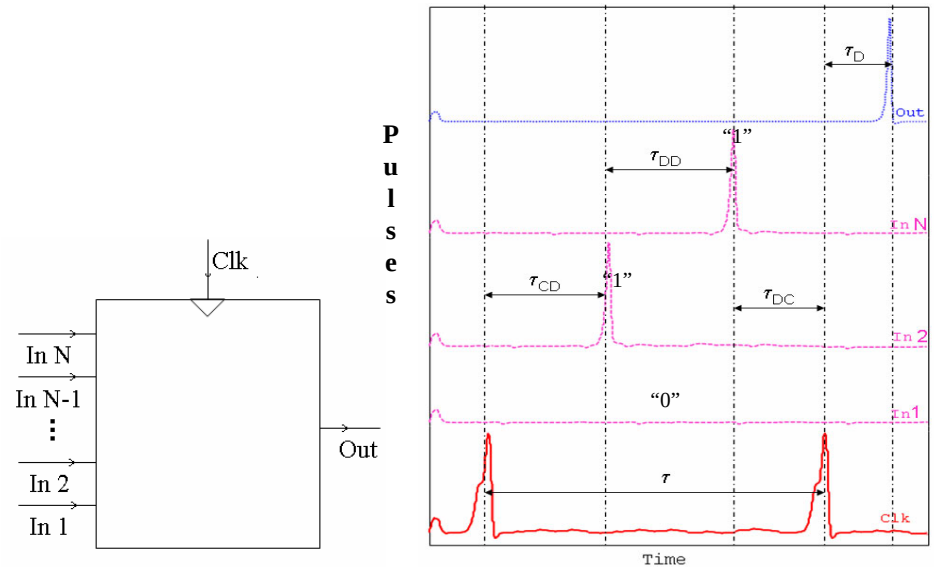

Figure 2.4: Protocol for RSFQ circuits: a) arbitrary logic block and b) timing parameters (not to scale).

Examples of the first group are the JTL, Splitter, Merger [7] etc. while AND logic gate, OR logic gate etc. belongs to the second group. The signalling protocol in RSFQ circuits have to be defined as it differs from that in conventional combinational logic as accepted in semiconductor electronics, because of the following two inter-related factors:

- "return-to-zero" nature of SFQ pulses,
- natural internal memory of quantizing SFQ loops.

Most RSFQ circuits implemented so far have been based on the standard RSFQ protocol illustrated schematically in Figure 2.4. An N-input logic box is given as example in Figure 2.4a. In this system, a signal in a data line is treated as binary "1" if it carries an SFQ pulse within the given clock period (signal "In 2" and "In N" in Figure 2.4b). The absence of the pulse during this time interval (signal "In 1" in Figure 2.4b) is interpreted as binary "0". More generally, any RSFQ circuit using this protocol can be considered as a connection of asynchronous components and clocked gates ("elementary cells" or "logic latches"). Such a gate has a few (typically two) internal states and may be functionally considered as an explicit or implicit integration of combinational logic and a latch. Input SFQ pulses change the state of the latch which stores this information until the arrival of the clock pulse. This pulse triggers output signal(s) and resets the cell into its initial state. As evident from Figure 2.4b, clocked flip-flops and logic gates cannot be fully characterized (as asynchronous components) by just the delay τ_D between the input (in this case clock) pulse and the output pulse; at least three more time constants have to be included:

- τ_{CD} or clock-to-data interval; the minimum value of the interval between the clock pulse and the first data pulse ("In 2" in Figure 2.4b),
- τ_{DD} or data-to-data interval; the minimum value(s) of the interval(s) between the data pulses,
- τ_{DC} or data-to-clock interval; the minimum value of the interval between the last of the data pulses ("In N" in Figure 2.4b) and the next clock pulse, at which the device operates correctly.

Since the sum $\tau_{CD} + \tau_{DD} + \tau_{DC}$ defines the clock period, its minimum value determines the maximum clock frequency of the gate given by:

$$(f_c)_{\max} = \frac{1}{(\tau_{CD} + \tau_{DD} + \tau_{DC})_{\min}} \tag{2.14}$$

In all single-input gates, such as an inverter, the data-to-data interval is not defined. Moreover, some two-input gates, like the AND and XOR operate at an arbitrary data-to-data interval τ_{DD}. In these cases, the $(\tau_{DD})_{min}$ can be ignored and is set to 0 for calculations.

2.4 Design and Implementation of RSFQ Circuits

One of the primary problems in the development of large RSFQ circuits was the lack of appropriate design methodologies that effectively utilize computer-aided design (CAD) tools while providing direction for the development of new tools specific to this superconducting technology. It is debatable whether RSFQ circuits should be designed based on leveraging techniques developed for semiconductor circuits or whether completely new methodologies specific to RSFQ logic should be created. The proponents of the former approach affirm the analogies between both technologies, particularly strong at the system level, and stress the achievements and maturity of semiconductor technologies. The proponents of the latter approach stress the substantial differences between the two technologies, particularly strong at the circuit level, and the large difference in the operating speed, power consumption, and fabrication process. A combination of both strategies is probably the most effective methodology.

The design methodology for small-scale RSFQ circuits is centred around circuit simulation and the optimization of device parameters while the design methodology for large-scale circuits is focused on logic (gate-level) simulation and optimization of the interconnect delays within the circuit. The second important feature is the development of libraries composing of basic RSFQ cells, permitting the design of circuits of arbitrary complexity. This process of constructing large RSFQ circuits out of a general family of primitive gates has not been commonly accepted. The main obstacles with regard to this approach are:

• difficulty of isolating RSFQ gates from each other;

• large uncertainty of delays and other timing parameters of RSFQ cells due to variations in the fabrication process and changes in the bias currents;

• use of Josephson transmission lines (JTLs) for interconnects;

• low fan-out of RSFQ gates;

• lack of a well-established methodology for modelling the timing of RSFQ circuits;

• lack of tools for the timing analysis and timing optimization of RSFQ circuits;

• lack of tools to logically simulate RSFQ circuits.

The latter three obstacles are being dealt with by modifying and integrating the advanced CAD tools for semiconductors. The design of large RSFQ circuits is currently based almost exclusively on a full-custom methodology. This approach is justified by the immature state of RSFQ technology and by the niche applications of RSFQ circuits, such as time-to-digital converters [19] or decimation filters for analogue-to-digital converters [20], where the advantages in performance, in terms of both speed and power, are of primary importance. Nevertheless, this design style also leads to long design times and significant design effort. Further development of RSFQ technology and its application to digital signal processing [21] and general purpose computing [22], [23] requires adopting a more labour efficient and less error-prone semicustom design methodology. Unfortunately, differences between superconducting RSFQ logic and traditional semiconductor technologies prevent the direct application of semiconductor methods and tools to the automated design of RSFQ circuits.

The design flow of a small-scale RSFQ circuit consists of three main phases: synthesis of the circuit structure, optimization of the circuit parameters, and physical implementation of the circuit layout. This design flow is commonly accepted and supported by multiple commercial and public domain CAD tools [24], [25].

The synthesis of a small-scale RSFQ circuit begins with a description of the circuit function using a Mealy state transition diagram or present-state/next-state table. The circuit structure along with a set of near exhaustive input stimuli is used to verify the functional behaviour of the circuit which is derived from the circuit function. This step is currently not automated and is primarily dependent on the intuition of the designer. The circuit is simulated and modified iteratively to verify full functionality for all input sequences.

The custom optimization package is then used to determine the optimal nominal values of the circuit device parameters that achieve the maximum yield in case of parametric variation during realisation [26]. Before the optimization procedure can begin, a pass–fail criterion is generated to permit distinguishing between sets of operating parameters that give correct and incorrect circuit functionality. These criteria are generated automatically by simulating the circuit for the set of initial operating parameters. This pass–fail criterion only considers the externally observed behaviour of the circuit, i.e. sequences of pulses at the inputs and outputs of the cell.

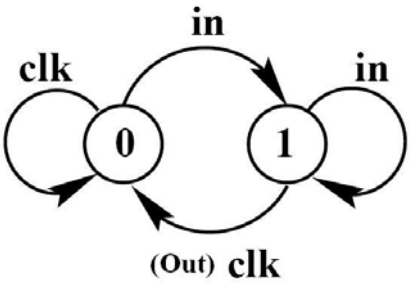

Figure 2.5: Mealy diagram for an RSFQ DFF.

After the optimum values of the device parameters are determined, the layout view of the cell has to be drawn manually. At this level of abstraction, the circuit is described in terms of the physical geometric data used to produce the individual lithographic masks. The layout data is then compared with the schematic and further fine tuning is carried out taking into account the parasitics. The next sub-section will illustrate the process using an RSFQ circuit example.

2.4.1 An RSFQ DFF

An RSFQ DFF, being a simple circuit, is used here as a design example. The Mealy state diagram for the RSFQ DFF is shown in Figure 2.5. If the circuit is in its "0" state, arrival of the "in" pulse will set the DFF to its "1" state. Arrival of a "clk" pulse at this state will release an SFQ pulse to the output of the circuit (shown in the brackets) and resets the DFF back to the "0" state. If a "clk" pulse arrives in the "0" state or if an "in" pulse arrives if it is in the "1" state, the DFF circuit will remain in its original state.

L1 = 2.74 pH
L2 = 6.075 pH
L3 = 1.975 pH
L4 = 1.064 pH
J0 = 0.2375 mA
J1 = 0.2375 mA
J2 = 0.185 mA
I_b = 0.125 mA

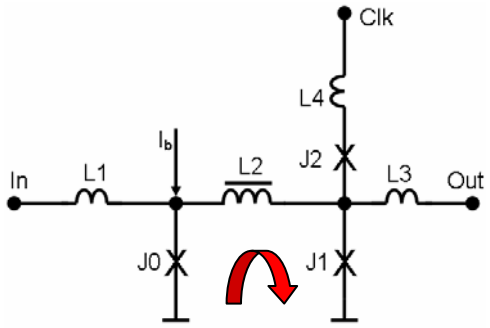

Figure 2.6: An RSFQ D-type Flip-flop with optimised circuit parameters.

The circuit schematic of the DFF is shown in Figure 2.6. It consists of three JJs (J0-J2), 4 inductors (L1-L4) and a bias current source, I_b. The storage inductor L2 (inductor with a line over it) forms the storage loop with J0 and J1 (shown by the arrow). The JJs, J1 and J2 form the decision-making pair in the circuit. This circuit has been optimised at Chalmers University in Sweden [27] for the HYPRES Nb process described in the fourth chapter of this thesis. The maximum frequency of operation is 20 GHz at a temperature of 4 K.

The operation of an RSFQ DFF is as follows. Arrival of an SFQ pulse at the "In" node will switch the junction J0 and a magnetic flux quantum (fluxon) is stored in the loop containing L2. Arrival of a pulse at the "Clk" node will switch either J1 or J2 depending on the state of the storage loop. The critical currents of J1 and J2 are designed such that if a fluxon is present in the storage loop, J1 will be switched releasing the stored fluxon to the "Out" node. If a fluxon is not stored in the loop, J2 will be switched instead of J1 and there will be no emission of a fluxon to the "Out" node.

The layout of the discussed DFF circuit is given in Figure 2.7. Inductors are realised by using metal wiring layers and metal layers are also used for the distribution of bias current (I_b). The first metal layer is used as ground plane to achieve circuits with better performance. The square boxes (a) are moats (holes in the ground plane) to avoid flux trapping in RSFQ circuits. Flux trapping is the phenomenon in which an unwanted fluxon gets trapped in one or more of the JJs or storage loops in the circuit, when the chip is being cooled down to 4 K. This DFF design will be used for the verification of the fault models in Chapter 6 of this thesis.

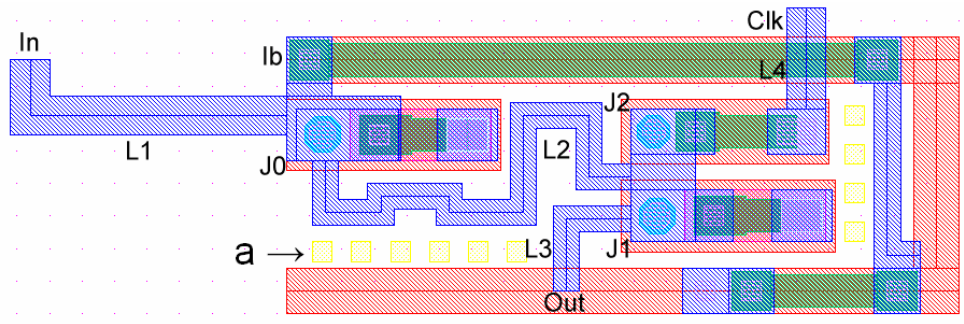

Figure 2.7: Layout of the RSFQ DFF designed in the HYPRES Nb process.

2.4.2 Josephson Transmission Line (JTL)

A JTL is the simplest available RSFQ circuit cell [7]. It allows an SFQ pulse to pass through it with possible shaping of the pulse and a short delay. The circuit diagram of a two-element JTL is shown in Figure 2.8. One element consists of J0, I_{b1}, L1 and L2. The second element is J1, I_{b2}, L2 and L3. L2 is being shared between the two elements. None of the inductances is capable of storing an SFQ pulse, hence transmitting it through the JTL.

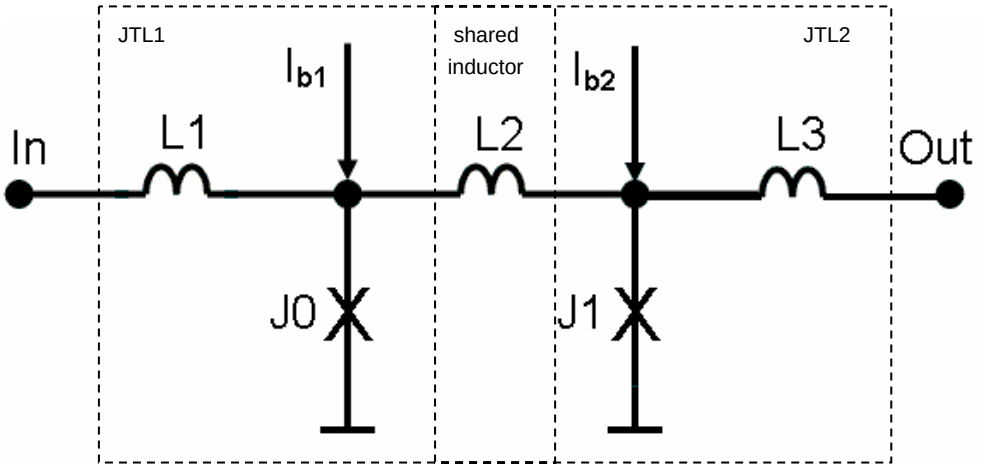

Figure 2.8: Circuit schematic of a two-element RSFQ JTL.

2.4.3 RSFQ Splitter and Merger

An RSFQ splitter and a merger are two other circuits used in the succeeding chapters of this thesis. An RSFQ splitter produces two SFQ pulses (one at each output) for a single incoming pulse and can be used to solve the fan-out problem in an RSFQ circuit. The circuit diagram and the symbol for a splitter is shown in Figure 2.9a. A merger on the other hand, produces an SFQ pulse at its output for every pulse at either of its inputs. The schematic and symbol are given in Figure 2.9b. A simple pulse multiplier is shown in Figure 2.9c to illustrate the operation of the circuits. The “D” denotes a delay segment which can be a JTL or a DFF. Figure 2.9d shows the output of the JSIM circuit simulation of the multiplier as well as the internal nodes. The previous circuits are used in the next chapter to illustrate the insertion of Design for Test (DfT) circuits into an RSFQ circuit.

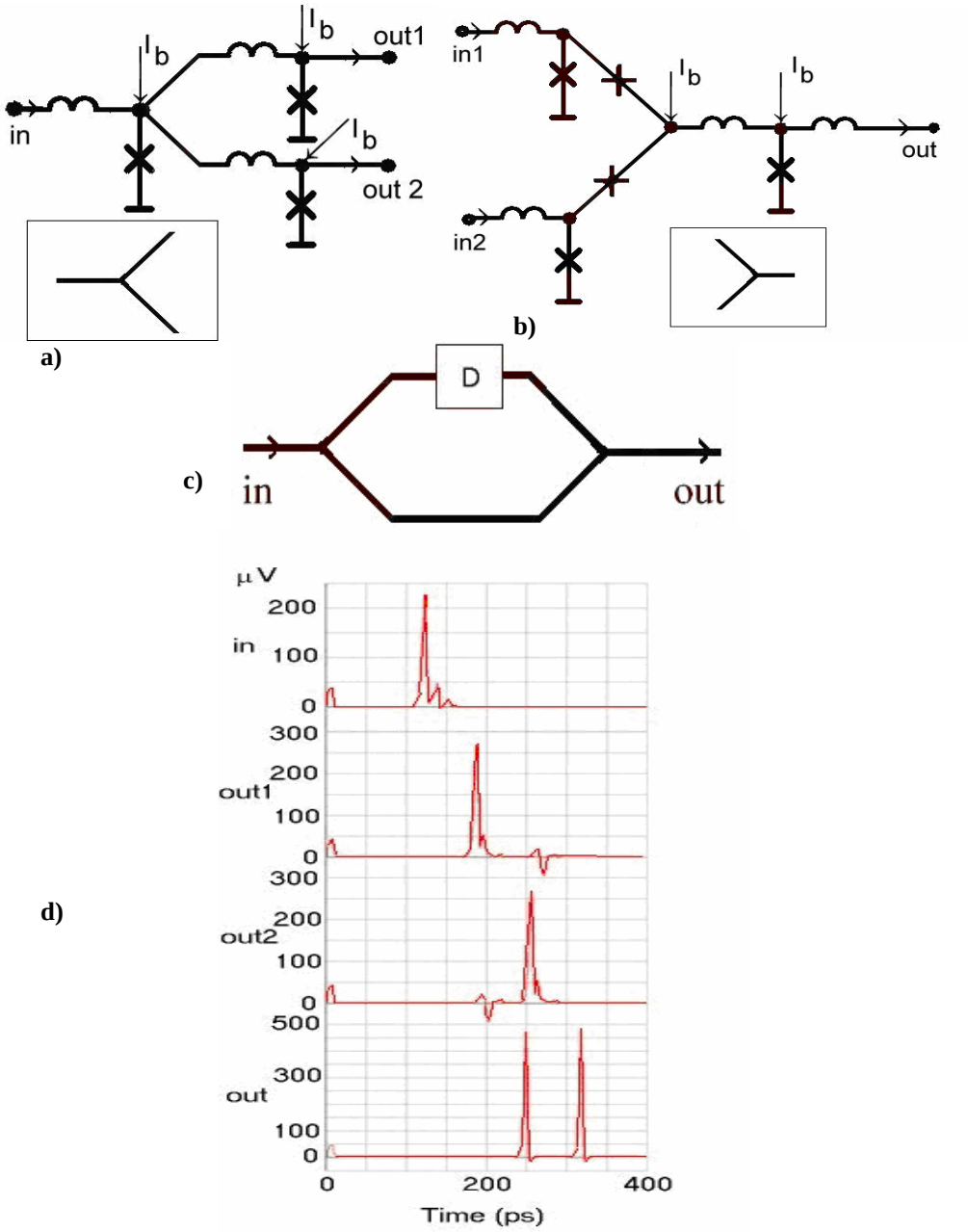

Figure 2.9: Circuit schematic of a) an RSFQ splitter, b) a merger, c) a simple pulse multiplier and d) JSIM simulated output of the multiplier.

2.5 Advantages and Disadvantages of RSFQ Circuits

RSFQ circuits can perform logic and arithmetic functions at extremely high (sub-terahertz) clock frequencies, just a few times lower than the maximum internal speed of the superconductors employed. These circuits represent the fastest digital technology currently available. Other advantages of this technology include:

- need for only a DC power supply;
- small power consumption virtually eliminating self-heating problems up to the VLSI level, at least for LTS circuits. Power consumption of RSFQ cells is not determined by energy dissipation inside the JJs (which is typically as low as ~10^{-18} joule/bit), but by dissipation in the DC supply resistors, and is of the order of 1 microwatt per gate [28], i.e., considerably less than that for latching logic (also compared to semiconductor counterparts) According to the 2005 International Technology Roadmap for Semiconductors (ITRS) prediction, even in the year 2016, RSFQ will outperform Si CMOS by a factor of two in energy dissipation [29]. This fact is also promising for the eventual transfer of this technology to higher temperatures of ~30K, using high-Tc JJs [28];
- natural self-timing (asynchronicity) which enables one to retain ultra-high operation speed in some important VLSI circuits, notably digital signal processors.
- natural quantum limited sensitivity of the SFQ pulses.

These impressive advantages do not mean that RSFQ circuits are free of problems. But one should distinguish fictional problems (as advertised in some publications) from the real ones. One of the claims was that one could not avoid the effects of the parasitic flux trapping in superconducting thin films, especially in the ground plane, of an integrated RSFQ circuit. However, the experience of teams that worked on the IBM and MITI projects show that this problem can be solved by fairly simple magnetic-field shielding. Furthermore, the usage of moats (holes in the ground plane) is an effective remedy towards stray flux [30].

Another argument is that the low amplitude (a few hundred microvolts) and short duration (a few picoseconds) of SFQ pulses would make fast communication between RSFQ circuits and a semiconductor electronic environment impossible. In fact, the existing SFQ/DC converters can deliver several hundred millivolts of DC voltage at their outputs in just a few tens of picoseconds. There are no problems in the development of special superconductor drivers which would raise the output voltage to ~10 millivolts in a few hundred picoseconds and semiconductor amplifiers with similar speed are capable of reliable readout of these signals. A 60 Gb/s communication between digital superconductor chips mounted on a passive carrier, using a novel driver circuit that produces a double-flux-quantum pulse were reported thereby answering various practical questions pertaining to chip-to-chip and on-chip communication in greater detail [31]. A high-speed output interface for an SFQ system has been demonstrated with an amplitude of 1 V at 10 Gb/s

[32]. The interface consisted of a Josephson latching driver, a room-temperature semiconductor amplifier, and a decision circuit module.

A real problem awaiting a solution is the DC power current recycling [33]. While the DC current necessary for powering of a single RSFQ device is quite modest, of the order of 100 μA per Josephson junction, the total current necessary for powering a VLSI RSFQ circuit may be much higher than the value which can be comfortably passed into a Helium cryostat by simple copper leads (a few amperes per lead). Hence, the DC current has to be "recycled", i.e. used for powering several fragments of the circuit. For this purpose, the fragments should be connected in series for the DC current, excluding the usual (galvanic) means of signal transfer between them. Work is being carried out in this area [33].

Testing tools also need additional development. As a typical example, the present state-of-the-art in SCE (complete system) is an automated multi-channel circuit tester OCTOPUX which can perform measurements of a diced chip at a rate of up to 300 kHz [34]. The developed software support of this system allows relatively sophisticated measurements of RSFQ circuits; for example, statistics of parameter spreads and thermal noise may be studied automatically with good accuracy using a special RSFQ circuit with only a few contact pads [35]. RSFQ circuit testing at multi-GHz frequencies can be carried out using special RSFQ on-chip test hardware [36] - [38]. Because of the unique speed of RSFQ devices, their testing by the available high-speed room-temperature equipment, which can only be extended to a few GHz, is hardly worth the effort as they are very expensive and not capable for the required "at-speed" test. Still, tools and methodology for comprehensive testing of RSFQ chips before wafer dicing have to be developed so that commercial production can be carried out [39], [40].

Another real problem that has to be dealt with is the necessity for liquid Helium cooling of LTS RSFQ circuits. Despite recent progress in closed-cycle cryocooler technology refrigeration, this may create serious problems for some potential users [41], and one needs to have a sizable circuit performance advantage in order to justify the related efforts. Ideally, SCE suits best for applications requiring ultra high-speed switching and large-volume data processing per unit time, where other technologies are far behind in their performances.

Yet another major problem is the absence of large JJ memories. Demonstrated RAM chips have shown a decent access time in the order of 400 ps, but only of a few kbit size [42]. Recently, Josephson hybrid RAMs have been investigated and the Japanese group at the Superconductor Research Lab has developed a 256-bit superconducting latching/SFQ hybrid (SLASH) RAM block as the first step in developing a 16-Kbit SLASH RAM, which enables high-frequency clock operation up to 10 GHz. The SLASH RAM is composed of AC-powered latching devices and DC-powered SFQ devices [43]. Yet another type of hybrid with CMOS is also under feasibility studies. The Berkeley cryo-electronics group has implemented an ultra high-speed interface circuit to amplify millivolt-level Josephson input signals to volt-level signals for CMOS circuits. The interface circuit includes a Josephson series-array pre-amplifier and an ultra-fast hybrid Josephson-CMOS amplifier. The main idea is to use high-density charge-storage MOS cells as the memory with CMOS

address buffers and decoders, and to access the output by high-speed, extremely low-power, superconductive detectors. This combination takes advantage of the best features of each technology [44].

2.6 Conclusions

This chapter discussed SCE to give a detailed introduction in RSFQ circuits. A JJ was described with associated theory behind its operation. The JJ model used in the simulator used in our research work was also presented. RSFQ logic using logic protocols was subsequently described. Design and implementation of RSFQ circuits with the example of a DFF was discussed in detail. The presented DFF will be used in Chapter 6 to enumerate defect-based testing of RSFQ circuits. Finally advantages and disadvantages of RSFQ circuits have also mentioned pointing towards the latest developments. Nevertheless, as presented in chapter 1 of this thesis, RSFQ finds its application for high-end computing and communication requirements.

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Chapter 3

Test Techniques for VLSI RSFQ Circuits

This chapter starts with an introduction to Integrated Circuit testing. Structural and Defect-Based Testing (DBT) is elaborated followed by a selection on test structures for fabrication process analysis. Various types of structures are treated and the measurement technique used for them is explained. The application of these test methodologies to an RSFQ process is subsequently discussed. Design for Testability (DfT) for RSFQ circuits is presented with possible structures for the defect-based testing of RSFQ circuits.

3.1 Introduction

For delivering high-quality electronic devices, it is essential to verify the quality level of the production process. In the case of an IC, extensive testing techniques performed at various levels of the process aiming that defective ICs are not delivered to an end-customer. In general, various levels of testing can be identified. One type is to verify whether the designs (devices) have met the design specification in their application. This is called application-mode testing. If the verification of the functional specifications is carried out, one refers to another level called functional testing. And if the approach is to verify whether the devices have met their structural specification, it is called structural testing since they depend on the specific structure (interconnects, netlist etc.) of the circuit.

In this thesis, structural test methodologies for digital RSFQ circuits are being dealt with. Automatic Test Pattern Generation (ATPG) for RSFQ circuits is the ultimate goal. Until now, only functional approaches were used for the verification of the circuits. For employing structural-based testing, structural information is required about the devices under test. This chapter deals with the structural test methodology applied to RSFQ circuits.

SCE is emerging as a technology for solutions in high-end applications in computing and communication. In systems consisting of several thousands of gates, the trend is to introduce certain testability options at the design phase. Main goal of this Design for Testability (DfT) approach is to make the system testable, lower test costs, and reducing the test-time by increasing the ease of testing. This is desirable, as the system under study is complex; hence it is not possible to test all components directly within the system.

A DfT-based approach is essential for commercial production of complex reliable systems in SCE. As the complexity of the system increases, testing becomes complex and if not properly addressed, the system becomes non-testable. Hence complex systems should be designed with testability in mind. The design-for-test structures should be able to detect the faults in the system under study. Controllability and observability are the key features for DfT.

The organisation of this chapter is as follows. Section 3.2 deals with IC test methodologies. Structural and defect-based testing as well as DfT is described in this section. Fabrication process analysis is described in Section 3.3, while methodologies for the determination of structural defect distributions are presented in Section 3.4. Application of the process test methodologies to SCE is presented in Section 3.5. Finally, a DfT approach for RSFQ circuits is described in Section 3.6.

3.2 Methodologies for IC testing

Testing is the experimental analysis of a system consisting of the following:

1. Application of certain signals called test vectors to the system under study
2. Receiving the response signals for the test vectors from the system

3. Comparison with the expected result and ascertain the correct operation.

If the correct behaviour is not observed, investigation for the cause of misbehaviour is carried out called diagnosis and appropriate corrective measures are taken.

As mentioned before, various test methodologies are applied to ICs. Along with the progress of IC technology, associated testing methodologies were developed to verify the realised design [1]. A defect is a deviation of the physical parameters of the structures of an IC from the properties predicted by its design. A fault is a defect that causes the results of the electrical measurements of the IC structure to differ from required parameters resulting in malfunction. Detection of the nature and cause of the fault in the realised circuits is important for the commercial release of a product. A systematic test methodology is essential as direct monitoring of the internal nodes in an IC is not possible due to the unfavourable ratio of input-output (IO) pins and internal nodes.

The tests performed on an IC can be divided into two main categories: functional and structural. Functional testing deals with those techniques that are used to test the device by verifying its functionality. In functional testing, test vectors are applied while the system is in its normal operating mode. Special hardware modification in the device is not required. Structure-specific analyses of the circuits are conducted while employing structural testing. Introduction of additional circuitry is often required while performing structural testing. In practice, both the functional and structural aspects are sometimes intermixed for better testability.

For digital ICs, functional testing is often simple and straightforward. But it is time consuming and the faults are often indistinguishable while employing functional tests. Furthermore, detection of the nature and cause of the fault is not possible using functional tests. Implementation of the test routines can be expensive as the price of Automatic Test Equipment (ATE) is related to the number of IO pins and the operating speed. Additionally, it is impractical for the ATEs to keep-up with the operating frequencies of the devices, making them unsuitable for at-speed testing as the operating frequencies of the devices are rapidly increasing.

3.2.1 Structural and Defect-Based Testing

For structural testing to be carried out, a systematic methodology has to be developed. Information about possible defects in the technology is gathered and fault models are developed for different probable faults. Specific test patterns are developed after a careful study of the structure/topology of the circuit. Tests are carried out for a specific set of faults using the available fault models. Hence, the nature and cause of the detected fault is known or can be determined using the available diagnostic methods. Another major advantage of structural testing is that expensive ATEs can be sometimes replaced with less expensive ones. However, an at-speed testing of the device is not always possible.

Knowledge about probable defects and their statistics is an essential factor in carrying out structural tests. Information about random spot defects, occurring random in nature, is

important because they contribute to the majority of the defects in a mature process. The most common physical defects that occur are shorts and opens in wiring layers, resistive via defects and pinholes in oxide layers. Cracking of metal layers is another issue, which, in the worst case, can become an open in the layer.

The effective detection of these defects in a manufacturing process are carried out using specially designed test modules also called Process Defect Monitors (PDM) [1], which consist of a number of test structures. Of the different kinds of PDMs, those used for the determination of the structural-defect distribution (short, breaks etc.) is useful for our study on structural testing. The information gathered using these structures is the basis for Defect-Based Testing (DBT) [2]. Inductive Fault Analysis (IFA) [3] is a widely used technique for DBT. It is based on the fact that the probability of a defect occurring is a function of the local *layout* geometry and the *distribution of defect mechanisms* observed from the manufacturing process. It should be noted that the presence of defects in ICs does not necessarily mean that they do not fulfil the technical requirements. Only those ICs are faulty in which defects are found in critical regions making them non-functional. This means that certain ICs having defects will function well like a defect-free one as long as they do not occur in the critical parts of the IC.

A defect ranking is used to create a realistic fault list. Faults are resulting from defects that cause malfunctioning of the realised circuit in the technology under study. Fault models are then developed to translate the defect information into the circuit under study for simulation and test generation. In IFA, the defects are sprinkled virtually on a fault-free layout according to the probability distribution of defects. Then, a detailed simulation of the circuit performance is carried out to evaluate possible faulty circuit behaviour. This results in a set of test vectors, which are capable of detecting a set of specific faults. The procedure is called test-pattern generation. For ATPG, special algorithms have been developed to generate the test vectors automatically based on verified fault models and logic circuit topology. Fault coverage refers to the percentage of the possible faults detected by a certain test vector generated by applying a particular fault model.

3.2.2 Design for Testability

A fault, like a stuck-at fault, is said to be testable if there exists a well-specified procedure to expose the fault, which is implementable with a reasonable cost using current technologies. Similarly a circuit is testable with respect to a fault set when each and every fault in this set is testable. Testability can be described as the ease with which the functionality of the circuit can be determined to a desired degree of accuracy. Design for Testability (DfT) [4] refers to those design methodologies which put constraints on the design process to make test generation and application cost-effective.

Those efforts include maximising the fault coverage, minimising test-generation effort and test-application time. In general, by means of DfT, controllability and observability of the design is improved. Controllability is the ability to establish a specific signal value at each node in a circuit by setting values on the circuit’s input. Observability is the ability to

determine the signal value at any node in a circuit by controlling the circuit's input and observing its output.

There are two classes of DfT techniques – ad-hoc techniques and structured techniques. Ad-hoc techniques include good design practices learnt through experience and design reviews conducted by experts or design auditing tools [4]. Structured techniques include scan and Built-In-Self-Test (BIST) designs [5].

As mentioned before, controllability and observability are the key terms related to DfT. This is often achieved by either a re-synthesis of the existing design or the addition of extra hardware in the design. Most approaches require circuit modifications and factors such as chip area, IO pins and delay times are affected. Usually these factors increase if DfT techniques are applied. Hence a critical balance exists between the attainable gain and the applicable DfT. If the chip area increases, the probability of defects in the chip increases thereby reducing the yield. If there is no appreciable increase in fault-coverage as a result of the DfT insertion, the defect level will be higher than in its non-DfT state because of yield issues. Due to this, a trade-off exists between the testability options and the cost.

3.3 Diagnosis of the IC Fabrication Process

The type of problems that can occur in an IC flow can be divided into two categories: design and process errors and manufacturing defects. In this thesis, only manufacturing defects will be considered. Due to the imperfections of the manufacturing process, various defects are present in real ICs. These defects can be classified into three subclasses [6]:

1. Gross manufacturing defects
2. Parametric defects
3. Structural (Random) defects

Defects that affect a large fraction of the fabricated ICs (e.g. a complete wafer) are called gross manufacturing defects. They are large deviations from the design resulting from serious operator error or major machine breakdown. They are rarely present in a mature fabrication process.

Parametric defects are those defects by which a portion of the wafer is defective due to the fact that the electrical parameters in that region deviate beyond the allowed margins of the designed values. In terms of dimensions, these defects are present in more than a single chip and they can be found in certain areas affected by the defect. They are caused either by the imperfection in the wafer/substrate or improper processing conditions. Parametric defects are mostly caused by non-uniformities of processing conditions over the wafer area. All ICs in the region where parametric defects are found is said to be faulty since they do not fulfil the technical requirements [6].

Structural (or spot) defects are resulting from discontinuous distributions of certain physical parameters over a wafer. They are also called random defects due to the fact that

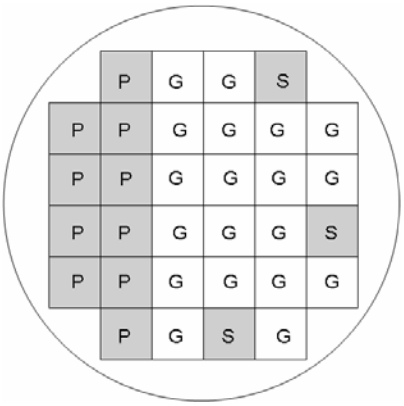

Figure 3.1: Wafer map showing the presence of defects in a process: G represents the good chips; P parametric defects and S spot (structural/ random) defects.

they occur randomly over the wafer area. In terms of dimension, they are present in an area smaller than a single chip and single chips are being affected by these defects. Major reasons for the presence of random spot defects are the presence of contaminating particles on the wafer or photo mask during processing, irregularities of the crystalline structure of the wafer and mechanical damages. Random defects are important because they contribute to the majority of the defects in a mature fabrication process. Figure 3.1 shows a sample wafer map showing the presence of parametric and structural defects; shaded portions in the wafer represent the defective chips.

The most common defects that occur in conventional CMOS IC technology are shorts between the same metal layer resulting from extra material (due to under-etching) and bridges between different metal layers due to the absence of an insulation material. In addition there are opens in layers or in vias resulting from the absence of conducting material or excess insulating material in the vias causing insufficient opening of contact windows. Another category is pinholes in oxide layers and metal step-coverage problems over under-lying layers [6].

The effective detection and avoidance of these defects in a manufacturing process is essential for the quality of the devices developed in that technology. Information about these defects in a process is gathered by using specially designed test modules called Process Control Monitors (PCM) [1]. Depending on the information that can be acquired, there are four types of test structures that can be used for:

1. Evaluating the functional properties of IC building blocks (test circuits)
2. Extractions of IC geometric parameters like specific dimensions
3. Determination of electrical parameters like the critical current, I_c.

4. Determination of the structural defect distribution and their influence on yield (short, breaks etc.)

Structures in the first group are electronic circuits similar to the one used in the IC block and are used to verify the functional behaviour of the IC building blocks under various conditions. The second type is designed so that their electrical parameters depend strongly on the dimensions of certain regions, e.g. active areas. The misalignments between different patterns and variation in the designed and realised geometries are detected using this type of structures. The third type of test structures consists of all structures which allow the determination of electrical and/or physical parameter values which are important in the manufacturing of the ICs. Critical currents and surface resistance measurement fall under this group in RSFQ processes. The fourth group are the structures that enable the determination of structural defect distribution and the influence of these defects on the IC building blocks. Shorts and breaks in conducting layers, contact resistance measurements belong to this group.

Until now, most research in superconductor processes has been done on parametric defects, in particular critical currents. As the processes become more mature, the importance of detecting the random defects increases. This is due to the fact that the occurrence of gross manufacturing errors and deviation of parametric values are decreasing due to the maturity of the process. However, random spot defects can still occur due to various reasons like the presence of impurities, local wafer defects. In this chapter, the fourth group of structures, i.e. those structures used for the determination of structural (random) defect distribution is treated.

After obtaining the defect statistics, the yield in the fabrication process can be determined by the following method. If a uniform defect density is assumed, the probability 'p_k' that a given chip contains 'k' defects is given by the binomial distribution [7]:

$$p_k = \frac{n!}{k!(n-k)!} \cdot \frac{1}{N^n}(N-1)^{n-k} \tag{3.1}$$

when 'n' defects are randomly distributed among 'N'chips. The yield Y is defined as:

$$Y = Y_0 \cdot Y_1(D_0, A, \alpha_i) \tag{3.2}$$

where (1-Y_0) is the fraction of chips that produce bad chips due to process variations or parametric defects and (1-Y_1) is the fraction of the remaining chip sites that produce bad chips due to random defects. Y_1 is a function of D_o, the density of defects; A denotes the area of the chip and α_i, the parameter unique for each yield model [6], [7]. Determination of yield from defect statistics, applying the available yield models is itself an area of research [8] and is beyond the scope of this thesis. That will be left as future work.

3.4 Determination of Random Defect Distribution

Special care has to be taken in selecting the test structures so that not more than one type of defect is detected and the critical areas in the structure should be comparable with the real situation in an IC. As mentioned in the previous sections, the main possible random defects in an IC manufacturing process are:

1. Intra-layer shorts and opens
2. Interlayer shorts
3. Step-coverage problems
4. Contact(-via) problems

Each of the mentioned categories is dealt in detail in the following sub-sections with the

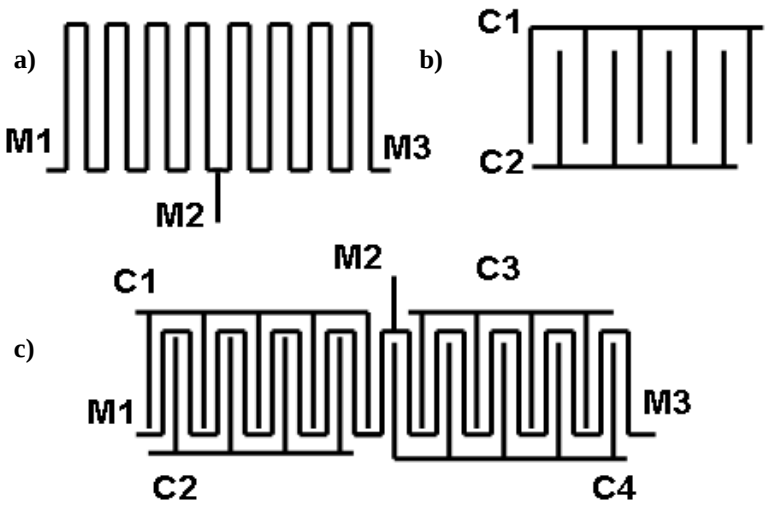

Figure 3.2: Structures for detecting intra-layer opens and shorts in a conducting layer: a) meander structure; b) comb structure and c) a comb-meander structure.

corresponding structures for defect detection in an RSFQ fabrication process. They have been adapted from semiconductor process to be used in an RSFQ process as described in the sub-sections.

3.4.1 Intra-layer Shorts and Opens

An *intra-layer open* can be determined using a meander structure [6]. The schematic of a meander structure is shown in Figure 3.2a. On measuring the resistance of the meander structure, in the figure, for e.g. between M1 and M3, any irregularities can be found. The design is carried out such that the wire width is according to the design rules and the separation between the wires is increased to avoid multiple-fault detection, viz. an *intra-*

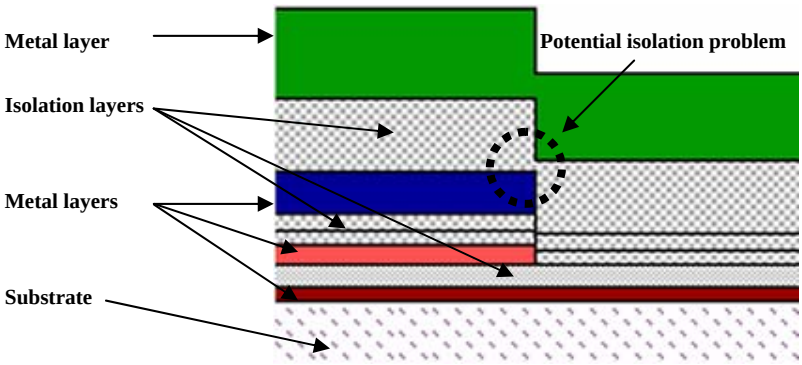

Figure 3.3: Cross-section of an RSFQ process showing the possibility for an interlayer short over an edge due to insufficient isolation material.

layer short. Design-rule exploration can be carried out by changing the wire-width of the layer under study. An intra-layer short can be also determined using the above described meander structure after modification. The separation of wires are laid according to the design rules and the wire-width is increased (more relaxed design-rules) to avoid the possibility of an open in the wire. Local taps like M2 in Figure 3.2a allows localisation of the defect in the structure and the number of structures between two taps is called a segment. More complex structures are available for the determination of intra-layer shorts. Figure 3.2b shows a comb structure that can be used for the detection of shorts. Minimum design-rule separation is held between the combs (for e.g. C1, C2).

Another structure that is used for detecting an intra-layer short is a combined comb-meander structure as shown in Figure 3.2c. This structure is an interleave of the meander and the comb structures. M1 - M3 is the meander and the comb structures are C1 – C4. The wire-width is such that the possibility of an open is avoided. Nevertheless, an occurrence of an unexpected open can be determined by measuring the resistance between the taps of the meander. As mentioned before, this allows the localisation of the defect in a long structure. The continuity of the meander is first measured by a four-point technique [9]. A short is detected if the measurement between any of the combs and the meander results in a measurable resistance.

3.4.2 Interlayer shorts

Interlayer shorts are caused by various reasons like a poor isolation layer or insufficient isolation material at an edge. Most often it is found in areas where the insulating layer has a stepped profile due to the complex underlying topology as shown in Figure 3.3. Here the probability of a short between the top metal layer and the lower adjacent layer is high due to the step in the former layer. This type of short is often formed due to damage of the photoresist layer used in lithographic processing. Hence, test structures with complex surface topographies are used to analyse this defect.

The probability of interlayer shorts are determined by placing the conducting layers over a large area to check the isolation integrity. A more efficient structure is to create similar topographical conditions as in Figure 3.3 to determine its probability. Since the probability of a step-coverage problem also increases with the complexity of the topology, special care has to be taken in designing the structures for the above defects to avoid detection of double defects. Special meander structures are used for this purpose. In the case of an inter-layer short test structure, the top metal layer in which the complex step occurs is reinforced by another conducting layer so that the probability of the step-coverage problem is eliminated. It should be noted that the additional conduction layer refers to a metal layer that is already present in the process but not necessary for the structure. This represents the normal layout of the structure to the defect under investigation but not making it non-sensitive to additional probable defects under normal conditions.

Figure 3.4 shows an example of a structure for detecting interlayer shorts in an RSFQ process. Figure 3.4a shows the placement of layers so as to create the required topology in the case of an interlayer short between the metal layers. Figure 3.4b shows the cross-section of a single segment in the structure. The influence of cracking in the top metal layer is prevented by adding an additional conductive layer over it. A measurable resistance between the different layers indicates the presence of a short between them.

3.4.3 Step-coverage problem

Another defect as mentioned earlier is the *metal step-coverage* problem. Due to complex steps in the underlying layers, the improper shape of the metal layer over the edges could lead to a crack in the layer. The effect of this will be an increased resistance in the wire due to the reduced cross-section formed by the crack or in worst case even a complete open. A schematic representation of a metal step-coverage problem is shown in

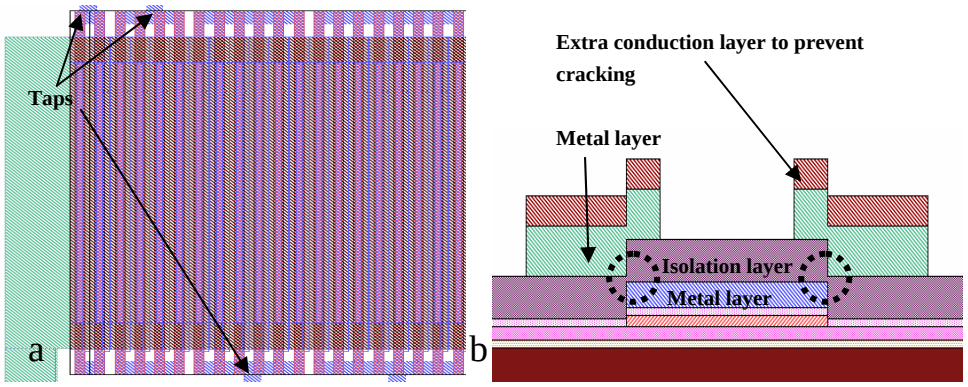

Figure 3.4: Structure for analysing interlayer shorts in an RSFQ process: a) overlay of layers to create the required topology and b) cross-section showing the presence of a second conducting layer to prevent the double detection of defect over an edge due to step-coverage problem (no process change introduced - see text).

Figure 3.5. Specific structures which emulate the critical step by introducing complex topologies are used for the determination of probabilities of these defects. In the case of a structure for step-coverage problems, additional conducting layers are avoided from the structure shown in Figure 3.4 so as to prevent a second conducting path in the structure due to inter-layer shorts. The reinforcing conducting layer which eliminates the probability of cracking is also removed in this case.

3.4.4 Contact (-via) problems

The next possible location for defects is a high contact resistance between layers at defective *vias*. A defect in a via could be due to either a problem with the contact window (for e.g. insufficient opening, misalignment etc.) or due to insufficient step-coverage of the top metal layer over the contact window. Hence, two types of test structures are used for the analysis. First type is a chain of contact vias. They are grouped into different sizes and lengths to determine the probability of occurrence (for e.g. a chain of hundred 2 x 2 μm via). The dimensions of the contact windows are made conform to the corresponding design rules used while other areas of the chain are made with relaxed design rules to prevent multiple-defect detection. For instance minimum-sized contact hole is made while the width of the meander wire as well as the separation between the meanders are increased to avoid open and short in the layers respectively.

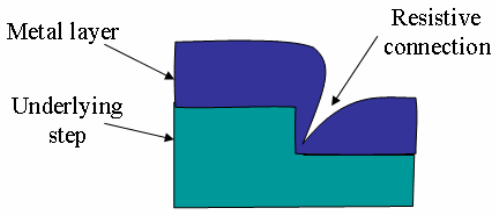

Figure 3.5: Increase of interconnection resistivity due to a metal step-coverage problem.

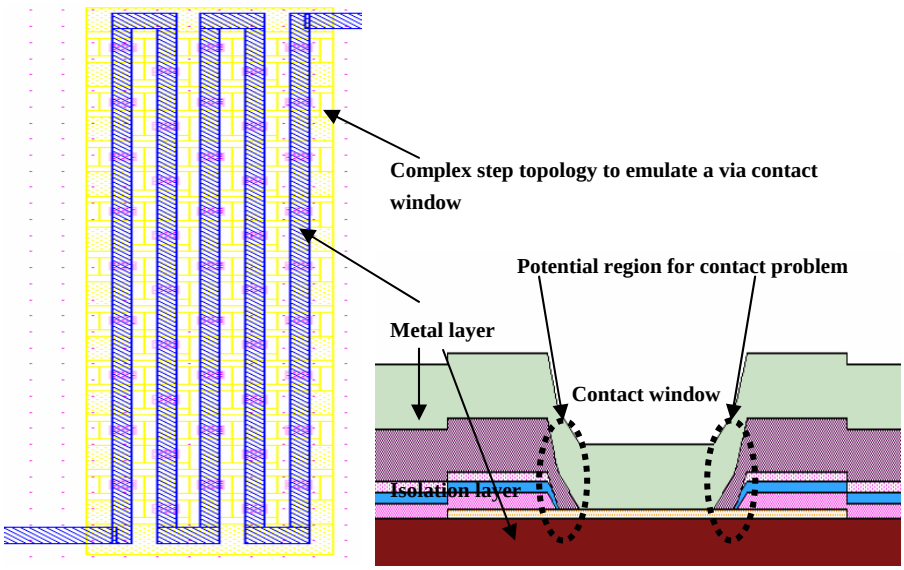

Figure 3.6: Structure for analysing step-coverage in vias in an RSFQ process: a) overlay of contact windows over a meander to create the required topology and b) cross-section showing the block metal layer under the contact window to prevent a second conducting layer.

The second test-structure type is an adaptation of the structure for step-coverage problems since the step-coverage of the top metal layer over the contact window is to be analysed. The improper shape of the metal layer over the edges of the contact window is one of the causes for contact faults. The metal layer is passed through several contact windows as shown in Figure 3.6a. Figure 3.6b shows the cross-section on an individual segment. The bottom metal layer is laid in blocks under the contact window in the structure to avoid a second conducting wire preventing the defect detection.

The method for determination of this defect is by simple electrical measurements as suggested in [10] and are called “van der Pol” structures. Such a structure is shown in Figure 3.7. The ratio of the resistance of the “stepped” meander wire is compared to that of the reference (non-stepped) meander wire. This ratio is used as a measure for the presence of defects near the steps. A four-point measurement scheme is implemented for this purpose to avoid contact resistance problems [9]. A current flow between points 1-3 in Figure 3.7 and the corresponding resistances of the reference and stepped meanders are measured between points 1-2 and 2-3 respectively.

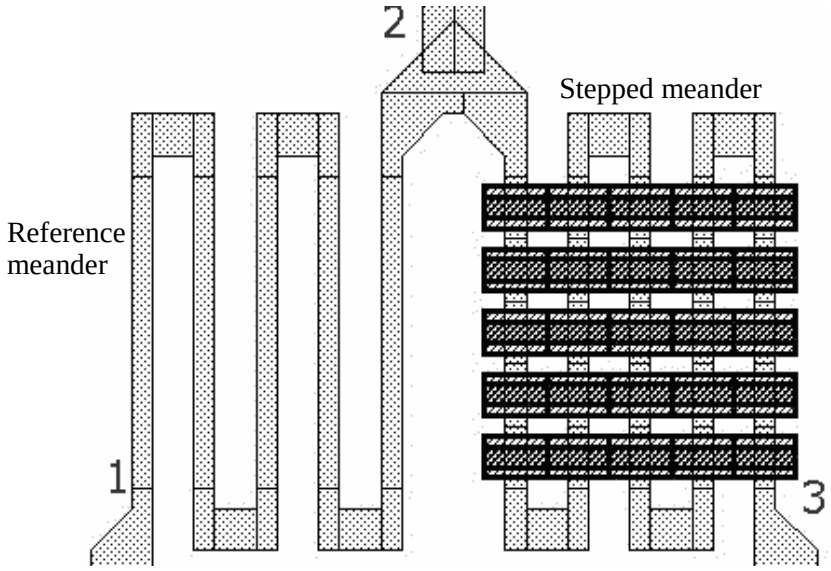

Figure 3.7: "Van der Pol" structure for localisation of defects by simple electrical measurements. The resistance of the stepped meander is compared to that of the reference meander to evaluate the influence of the steps in the layer.

3.5 Process Analysis of Superconductor Electronics (SCE)

A fabrication process analysis involves routine measurements. These measurements have to be carried out as efficiently as possible to reduce the test costs. Since RSFQ circuits work at 4.2 K, special measures have to be taken in testing them. Implementation of test schemes at 4.2 K involves additional costs. This is due to the fact that expensive cooling is required and measurements at 4.2 K are very time consuming. Additionally, the 4.2 K environment increases the complexity of the tests. Test-access mechanisms are still in their infancy and are currently limited to the available cryo-probes. Usually, the chips have to be wire-bonded and mounted on the cryo-probe before any measurements can be carried out.

An automated testing procedure is required to generate probability statistics for the process defects. However, for process-analysis testing at 4.2 K this is not a viable solution for reasons discussed above. It was concluded that all measurements to generate statistics have to be carried out at room temperature. Furthermore, translation of the measurement results at room temperature to low temperature is also crucial. Translation models were not available as well as only limited information about defects is available. Information about structures to determine the probable defects was also unknown. For the development of the structures, the idea to bring all measurements at room temperature was kept in mind.

Since interconnects behaves similarly in SCE as in the case of semiconductors at room temperature, those structures were adapted to analyse the available SCE processes.

In the case of a Josephson junction, special models were required. Historically, the quality of a JJ is determined using IV measurements on a series of JJs [11]. These measurements fall under the category of parametric testing. Adapting the existing measurement technique, a series of JJs could be used to determine the defect distribution in them. This method is based on the switching properties of the junctions and their highly non-linear IV-curve. Detection of possibly defective junctions in a series is possible. Defective junctions can have an IV-characteristic that is significantly different from the characteristics of a good junction [11], [12].

The most important measures found in literature [11] for junction quality are the critical current I_c and the V_m parameter. The V_m parameter, which is indicative for the subgap leakage, is said to decrease significantly in the presence of metallic impurities in junction barriers [11], [12]. The critical current is a crucial circuit parameter that can be influenced by for example reduction in junction area due to a defect. A parallel path model for defects suggested in [13], [14] supports that I_c and V_m can be independently influenced by a defect. A (physical) part of the junction behaves differently compared to the remaining good part of the junction. The parallel path model has been proposed for the case of pinhole defects. Pinholes have been shown to be inherently present in the thin AlO_x barriers of JJs [15], [16]. There are indications that they contribute significantly to the conductance of the junction (4-30%) [15]. They can be of sub-nanometre size and occur in the order of hundreds per square micrometer [13], [15].

It has been suggested in literature [17] that the switching properties of the JJs can be used to find a single defect in a long chain of series connected JJs. Based on this suggestion, a model has been developed by us that has helped to create a method for detecting and pinpointing possible junction defects [18]. As mentioned before, the method consists of an IV-curve measurement of several long series of JJs in a chain with taps as shown in Figure 3.8a. Several JJs are grouped together according to I_c values to make a sub-chain and several sub-chains makes a long chain which is part of the total chain of JJs. From the IV-curves it can be determined whether one of the long series possibly contains one or more defective JJs. Detection of defects by the suggested method in a JJ array is as shown in Figure 3.8b. Here, the dynamic resistance (the resistance at the reference point since AC is involved in the measurement: The ratio of the change in voltage to the change in current is known as dynamic resistance, DR = dV/dI) is plotted versus forced current for a series of JJs. The shown result is for a series of 320 JJs with two of them being defective (the designed I_c value of the JJ is 120 μA and accounting for the 20% allowed parametric variation good ones have a switching value between 196 and 144 μA). A JJ is said to be defective if its I_c falls beyond this limit.

A long series that is thought to contain a defect can be further investigated in detail by performing IV-curve measurements on segments of the long series. The procedure can be repeated down to a segment containing the minimum fixed number of JJs. A detailed analysis of our work is presented in references [18], [19], [20].

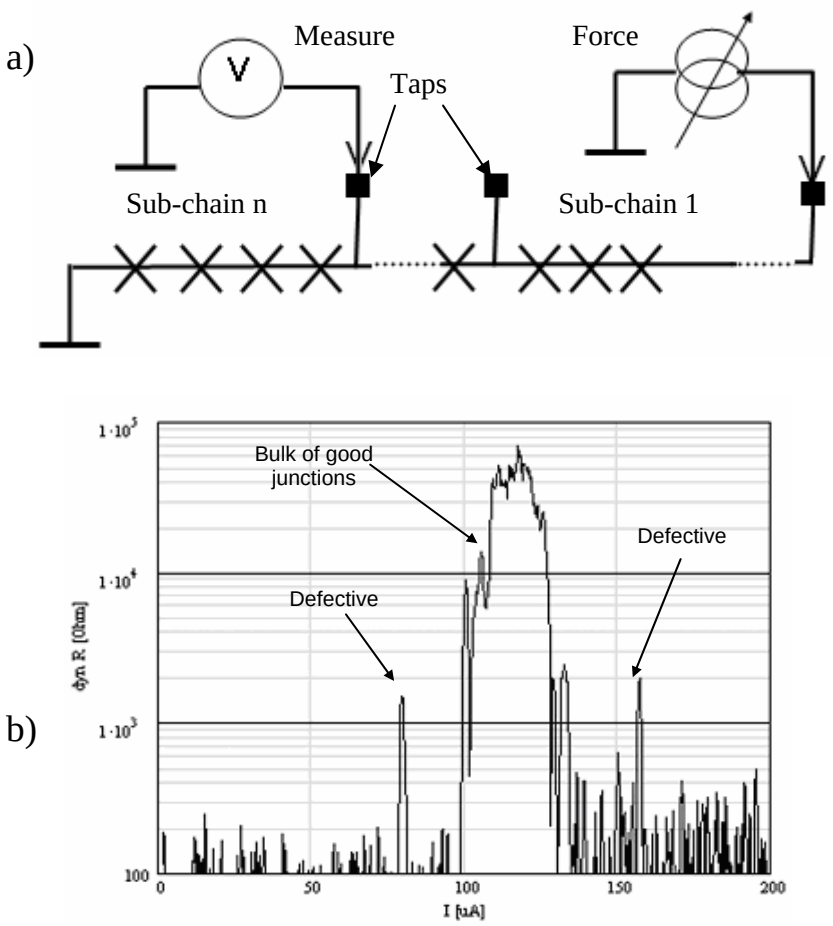

Figure 3.8: Analysis of a JJ: a) chain of JJs for localisation of defects by IV-measurements. b) Detection of defective JJs in a series: dynamic resistance versus forced current for a series of 320 junctions with two defective junctions (see text).

The previously described procedure requires several stages of measurement involving cooling. As mentioned before, this will be an extremely time-consuming task. Hence, a room temperature measurement for JJ structures is highly desirable. At room temperature, a JJ can be considered as a capacitor, since it is formed by the separation of two conductors by an insulating interface. Hence, a capacitance structure can be used to analyse defect in a JJ. Parallel to this, another group in MIT Lincoln Labs has proposed a Kelvin resistor for the determination of I_c at room temperature [21], [22].

Apart from these structures, certain support structures are required from the other type of test structures mentioned in section 3.3. These are the ones required for determination of electrical parameters for e.g. sheet resistance of a metal layer or the contact resistance between two conducting layers. For the measurement of a sheet resistance, a Greek cross

structure is commonly used [23] know as “van der Pauw” structure (this should not be confused with the “van der Pol” structure earlier described). An improved version of the Greek cross with a bridge for line-width measurement was presented in [24]. This structure is used for the determination of sheet resistance as well as variation of the line width from the designed values. Detailed investigation into RSFQ processes as well as specific structures will be presented in Chapter 4 of this thesis.

The results from the above mentioned structures serve two purposes:

1. Statistical information on defects for DBT and Yield analysis.

2. The determination of potential defect-prone areas to be monitored using a DfT structure in DBT.

As a part of DBT, various fault models have been proposed for SCE circuits, which will be presented in Chapter 6 of this thesis. These are theoretical models based on our work in structural testing and analysis of SCE processes [18], [19]. Until now, such models have not yet been verified. As the ultimate goal is to develop ATPG for SCE circuits to guarantee a high quality, verified fault models are required before going ahead with ATPG approaches. A test methodology based on a DfT approach is required for the verification of fault models. The fact that an individual Single Flux Quantum (SFQ) pulse is extremely difficult to be detected was hindering the verification process. A DfT scheme has been proposed by us to detect an individual SFQ pulse in reference [25]. In the following section, the DfT approach is described. Such a technique is applied in Chapter 6 to a simple RSFQ logic circuit to verify the proposed fault models.

3.6 DfT for RSFQ Circuits

Design for testability is a desirable option for SCE due to the fact that the circuits work at ultra-high frequencies and very low temperatures. Because of these operating conditions, the set-ups required for testing the realised circuits are bulky and expensive. Often the complex circuits turn-out to be hardly testable [26]. After realising this drawback, researchers have started working on testability of SCE circuits [25], [27], [28] but a DfT approach in SCE is still in its infancy.

Since DfT is a vast topic to be handled completely in this chapter, a possible technique will be elaborated using the example of SFQ pulse monitoring. It should be noted that the purpose of this is to be used as a tool for the DBT approach especially in the verification of fault-models developed for RSFQ circuits as presented in Chapter 6 of this thesis. The implementation shows how test points can be inserted into an RSFQ circuit [25].

Until now, tests carried out in SCE are mostly functional in nature. This is due to the fact that they are simple and straightforward to apply to these complex systems, once the (expensive) test equipment is available. But details of the defect that caused the fault in the device are not trivial using functional approaches. At this point a DBT approach becomes attractive. Nature and cause of the fault is sometimes deducible from the test vectors by observing their response by the circuit-under-test (CUT) using respective fault models.

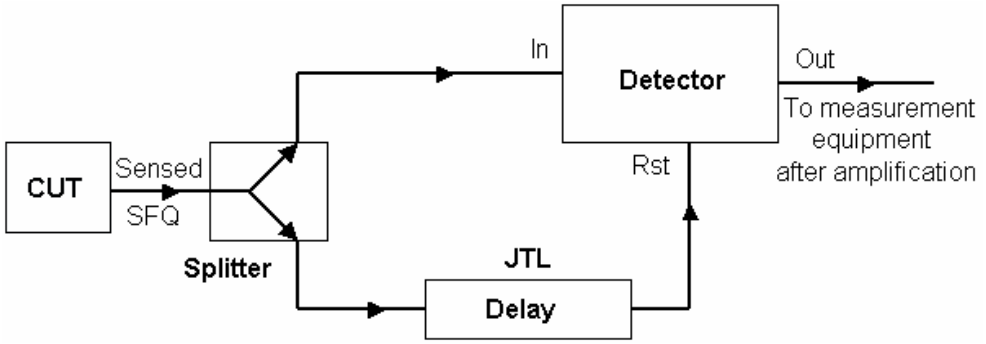

Figure 3.9: Block diagram of a DfT structure for monitoring SFQ pulses in an RSFQ circuit.

Monitoring nodes in a circuit, which are having a high probability of being faulty, is desirable while conducting DBT. These locations can be identified by the statistical analysis of the structures described in Chapter 4 of this thesis. It is extremely difficult to monitor an SFQ pulse in a circuit due to its basic properties. The monitoring of an SFQ pulse at an intermediate stage is important while applying a DBT methodology to SCE circuits. In this section, a scheme is proposed by which detection of an SFQ pulse inside a circuit is possible.

Figure 3.9 shows the block diagram of the proposed scheme. It consists of simple RSFQ circuit elements [29] like splitter, JTL delay line and a specially designed detector for the SFQ pulse. This structure is attractive in finding faults within a circuit where direct

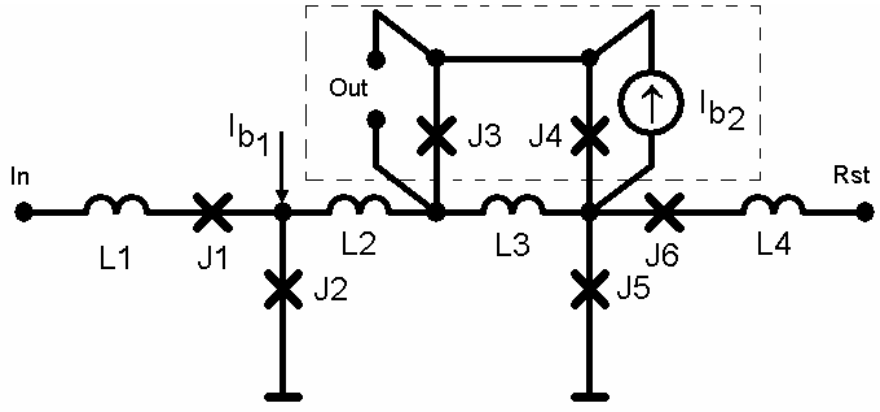

Figure 3.10: Circuit diagram of the detector used in the SFQ pulse monitor. Circuit parameters are (I_c of) J1 = J6 = 0.18 mA, J2 = J5 = 0.2 mA, J3 = J4 = 0.15 mA, (bias currents) I_{b1} = I_{b2} = 0.18 mA, L1 = L3 = L4 = 4 pH, L2 = 8 pH.

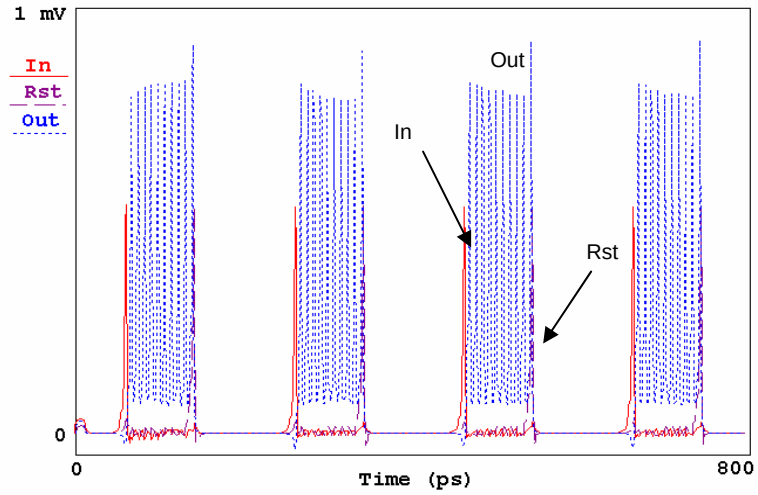

Figure 3.11: Simulated operation of the detector circuit designed for monitoring SFQ pulses.

external pulse monitoring is not possible. The SFQ pulse to be sensed is splitted and one part is applied directly to the input of the special detector circuit. The other pulse is applied to the reset input of the detector via a delay segment. By measuring the voltage at the output of the detector, the presence of an SFQ pulse can be detected.

The delay segment determines the duration of the voltage level at the output of the detector (Figure 3.9) as it determines the moment of reset. The delay can de made sufficiently long before the reset of the voltage state. As a result, less expensive external test equipment can be triggered using the amplified signal from the output of the detector. A JTL is used in the design to construct a delay line for this purpose. The output of the detector has to be amplified to be able for the external equipment to detect the signal.

The circuit diagram of the designed pulse detector is given in Figure 3.10. It is a

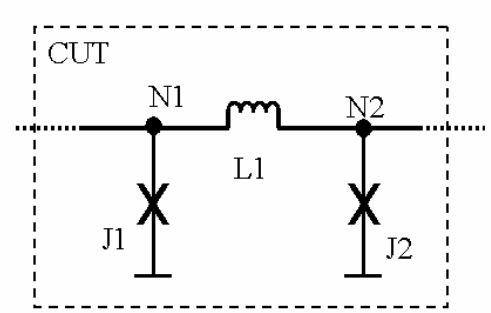

Figure 3.12: Schematic diagram showing part of the example CUT.

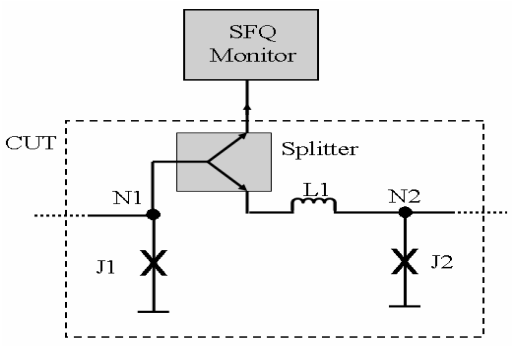

Figure 3.13: Schematic diagram showing the insertion of the monitor (DfT observation) into the circuit-under-test (CUT) using a splitter.

modified form of readout Superconducting QUantum Interference Device (SQUID) (A SQUID is a mechanism used to measure extremely weak signals.) [30] connected to a Set-Reset Flip-flop (SRFF) [29]. Arrival of an SFQ pulse on the "In" terminal will set the FF by trapping a fluxon in the J2-L2-L3-J5 loop. This in turn set the JJs, J3 and J4 into a sequential switching mode. The average voltage across the junction J3 can be measured after necessary amplification. This can be implemented on-chip or off-chip according to design specifications. Arrival of an SFQ pulse at the "Rst" terminal will reset the SRFF and the fluxon that is trapped escapes out of the loop. This in turn resets the sequential switching of J3 and J4, reducing the average voltage across them to zero. Figure 3.11 shows the operation of the detector circuit where a quasi DC value is measured at the output.

To illustrate the insertion of the DfT structure into a circuit, consider a part of an RSFQ circuit as example CUT (Figure 3.12). The part under study consists of two JJs, J1 and J2 at nodes N1 and N2 respectively and an inductance L1 between the nodes N1 and N2. In this

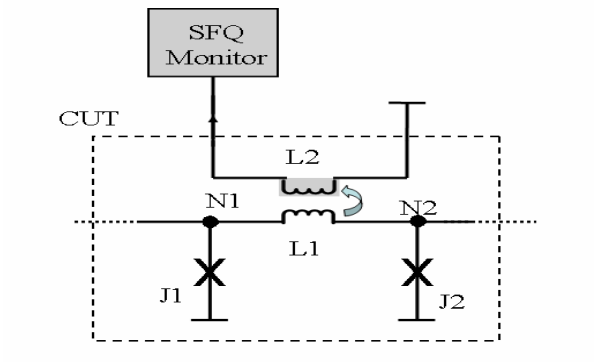

Figure 3.14: Schematic diagram showing the insertion of the monitor into the circuit-under-test (CUT) by a coupling inductance.

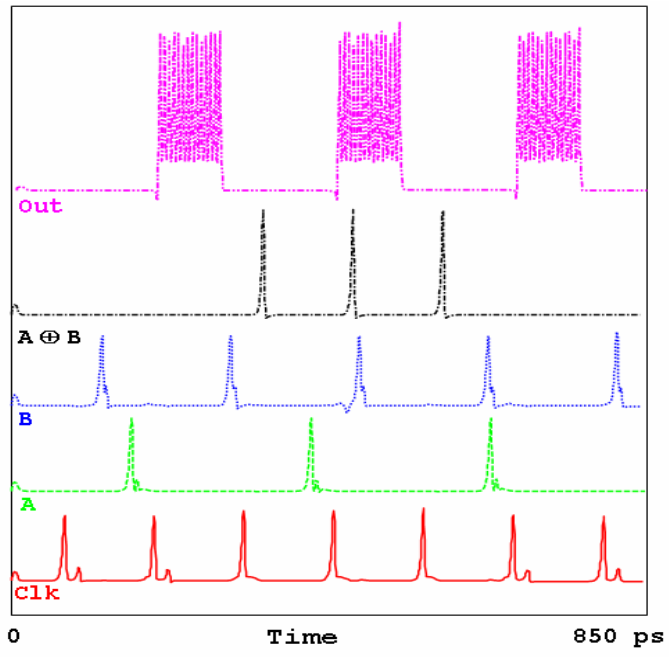

Figure 3.15: Simulated output "out" of the DfT monitor connected to one of the inputs (here input A) in an XOR gate circuit, the y-axis has been shifted for better readability.

case, the node that is to be observed is taken as N1. This can be approached in two ways. The first method is to use a splitter to insert the DfT structure into the CUT. The implementation is as shown in Figure 3.13; the additional DfT structure is shown shaded. The SFQ pulse arriving at N1 is splitted into two – one is fed back into the remaining part of the original CUT and the other to the input of the DfT structure.

This method introduces a delay in the original circuit, which is equivalent to that of the splitter (few ps). This has to be taken into account if the original circuit has a critical delay in the path in which the structure is inserted. This can be overcome by using the second technique. Here, an inductance is used to couple L1 to the DfT structure to sense the current flowing through it as shown in Figure 3.14. Special measures have to be taken so that no external current from the DfT structure flows back into the CUT through the coupling inductance L2. A unidirectional JTL [31] can be used if necessary in the design. All delays of the original CUT will now remain unchanged. It should be mentioned that L1 is a quantizing (storage) inductor which will enable the coupling of the flux to L2.

The proposed DfT structure was inserted into an XOR gate (not shown) as CUT, to verify the concept for a more complex circuit. The circuit was then verified using JSIM simulations. Various nodes were monitored and the results showed that the scheme is feasible. Figure 3.15 shows the simulation result of the monitor while using it to monitor an

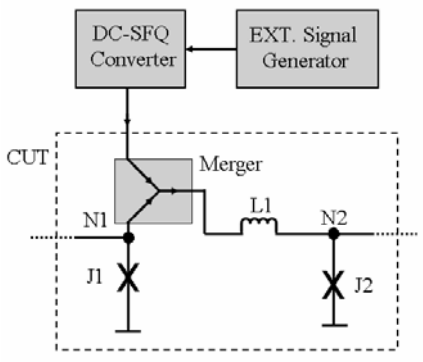

Figure 3.16: Schematic diagram of a DfT structure showing the insertion of test patterns into the circuit-under-test (CUT) using a merger from an external signal generator.

input node of the XOR gate. In this case, input A was monitored. This DfT scheme is useful, especially while conducting DBT for verification of fault models. Furthermore, only a few JJs are added by the DfT structure. This can be regarded as Test Point Insertion (TPI) to facilitate observability for RSFQ circuits.

Delay in the monitor can be controlled so as to customise the design for the measurement equipment. It should be mentioned that by using a similar approach used for the monitoring of the nodes, also test signals could be introduced into the circuit at a desired node. This is illustrated in Figure 3.16, in which a merger is used for TPI for controllability in the RSFQ circuit. Here the required test vectors can be applied to the CUT using an external signal generator through the merger. The limitations discussed earlier as in the case of monitoring circuit also hold here.

These approaches can be regarded as implementation of “primitive scan paths” for an RSFQ circuit, since the main idea in scan design is to obtain control and observability for flip-flops [5]. Further research is required to build-up this concept for RSFQ circuits as in CMOS. As said before, in our research it has been aimed for the verification of fault models. BIST will probably be the ultimate test solution for complex RSFQ circuits because of the complex test-access problems mentioned above [32]. The location for the DfT circuits in the case of a CUT is determined by analyzing the test structures developed for the technology in which the device is realised and the CUT topology. The following chapters will show how this is being carried out. The DfT structures can be used to monitor these defect-prone locations in a real circuit. This is required in a DBT approach, for the verification of the fault-models developed for RSFQ circuits. Fault models will be verified using the DBT methodology as presented in Chapter 6 of this thesis. Generation of the required test vectors for carrying out the structural tests will be available after the time-consuming IFA.

3.7 Conclusions

This chapter discussed Design-for-Test techniques for RSFQ circuits. A structural approach was presented for fabrication-process analysis. Several defect-monitor structures were designed for different types of probable defects in RSFQ process. Ease of measurement was kept in mind for the designs to bring about the measurements at room temperature. Special structures were also designed for JJs at LT so that comparison could be carried out for the translation of defects to RT. The presented defect-monitor structures can be used to gather statistical information, i.e. the probability of the occurrence of defects in the process. This forms the first step for IFA, a commonly used DBT methodology.

This chapter also discussed a possible DfT scheme for monitoring SFQ pulses within an RSFQ circuit. A DfT scheme is inevitable for RSFQ circuits because of their very high frequency of operation and very low operating temperature. It was demonstrated how SFQ pulses can be monitored at an internal node of an SCE circuit using TPI. The available features in the proposed design for customising the detector make it attractive for a detailed DBT of RSFQ circuits. A node control mechanism has also been illustrated. The test structures that were designed to determine the defect statistics in the process can also be used to locate the position for the insertion of the DfT structures. The DfT scheme has been verified by JSIM simulations.

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Chapter 4

LTS RSFQ Processes and Associated Defects

This chapter starts with a short introduction of superconductor processes used for RSFQ circuit realisation. Different types of processes are treated to get a general idea. Finally, the two LTS RSFQ processes which were investigated during this research work are presented in detail. A structural test methodology has been applied to both processes, leading to various probable defects that can occur. The classification of defects in an RSFQ process is also presented. Test structures were developed as part of the research so as to determine the defect statistics in these processes. This chapter concludes with the design implementation of test chips incorporating the above mentioned test structures.

4.1 Introduction

Every electronic circuit requires a technology for realisation. There are a number of processes developed for the realization of superconductor circuits. They are classified according to the type of formation of the Josephson Junction (JJ), the basic building block of modern SCE circuits. From the operation point of view, there are two types of processes viz. the Low Temperature Superconductor (LTS) and the High Temperature Superconductor (HTS) processes. As mentioned in the second chapter, a JJ is formed when two superconductors are separated by an interface. According to the nature of this interface, the fabrication processes is referred to as a superconductor-normal metal-superconductor (SNS), superconductor-insulator-superconductor (SIS) or superconductor-insulator-normal metal-insulator-superconductor (SINIS).

The requirement of liquid helium cooling for LTS circuits is considered as a disadvantage of using them. In 1987, the discovery of a superconducting compound (YBCO or $YBa_2Cu_3O_7$) with a transition temperature at 93 K [1] gave hope for HTS researchers as liquid nitrogen could be used for cooling. Ramp-type, intrinsic c-axis, grain-boundary, and step-edge etc. are types of Josephson junctions in HTS technology [2]. But until now, a reliable process technology for large scale circuits is not yet achieved for active HTS circuit fabrication. This is due to the fact that the process spread is much higher in an HTS fabrication process as compared to an LTS fabrication process. Hence, a reliable mass production of HTS thin-film device is not yet achieved. An in-depth treatment of HTS technology can be found in [2].

The organisation of this chapter is as follows. Section 4.2 deals with various LTS processes for the realisation of RSFQ circuits. The investigation conducted on the JeSEF process to detect the probable defects is presented in section 4.3, followed by the HYPRES process in section 4.4. The special structures designed for a JJ are presented in 4.5 and the implementation of the test chips in section 4.6.

4.2 LTS Processes for the Realisation of RSFQ Circuits

An SCE fabrication process is quite similar to that of a semiconductor process. In fact, an SCE process is much simpler due to the lower number of metal wiring layers. This is because complex systems can be implemented with a smaller number of the basic building block, a JJ, as compared to the number of transistors in semiconductors. For example, an 8-bit RSFQ microprocessor with a 167 million instructions per second (MIPS) speed performance consists of about 5000 JJs [3].

The normal substrate in an RSFQ process is an anodised Silicon wafer. A superconducting ground plane of Niobium (Nb) is deposited as the first metal layer. The first interconnect layer of Nb is deposited after the isolation layers. Then the JJs are formed followed by the resistor layer for bias and shunt resistances, each separated by its own isolation layers. According to the complexity of the process, the second and the third superconducting interconnect layers will be deposited following this step. Each isolation

layer has its own via definition for the interconnect. Finally, a gold layer is deposited for bonding access.

As mentioned before, the formation of the junction determines the JJ type. An Nb/Al/Nb Josephson junction is an example of an SNS junction [4] while an $Nb/AlO_x/Al/AlO_x/Nb$ is an example of a SINIS or a double barrier junction [5]. Due to the excellent tunnel characteristics of the $Nb/AlO_x/Nb$ SIS Josephson junctions [6], it has attracted many researchers and has been widely used for the fabrication of RSFQ circuits [7].

Literature supports this suggested fragile nature of the junction: pinholes and barrier inhomogeneities are thought to be the main cause for degraded junction quality and malfunction of junctions [8] - [10]. They have been shown to occur in very high numbers in oxides with thickness of a few nanometers. Reference [10] reports density of defects D, of $\sim 2.5 \cdot 10^{-3}$ μm^{-2} for 1.8 nm oxides and reference [8] reports about point contacts of the order of hundreds in a JJ with very thin (>1 nm) oxide barrier (D ~100 μm^{-2}). Even the smallest disturbances in the trilayer will drastically change the barrier performance [11]. Small contaminants in the vacuum or in the aluminum target during tri-layer formation may cause the barrier to grow incorrectly. Small physical deformations in the underlying layers can cause a junction and the barrier to deform. Roughness in the Nb base electrode or in the Al layer can cause conducting micro-bridges through the oxide layer. Also atomic interactions and crystal defects at the interfaces of the Al-oxide can cause degradation of the junction performance.

In this chapter, two SIS processes will be discussed. Investigations were carried out on the probable defects in these processes and the developed test structures will be described in the following sections.

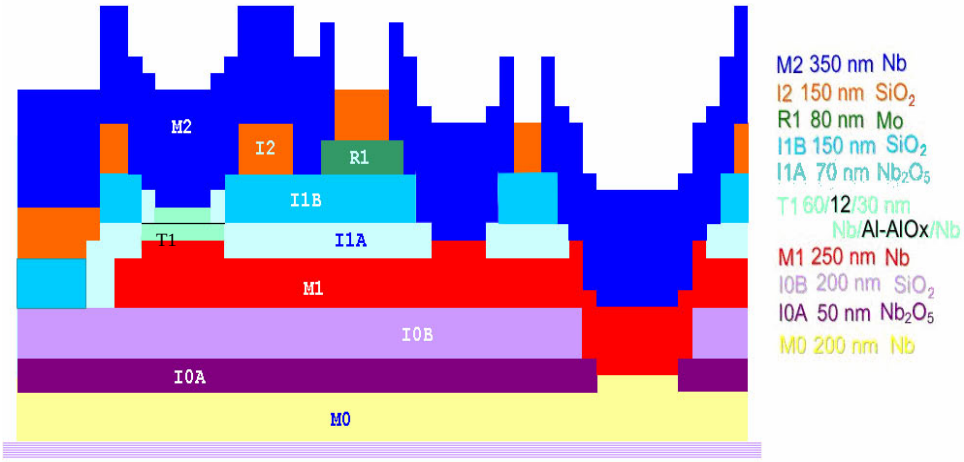


Figure 4.1: Cross section of the JeSEF Nb process.

4.3 The JeSEF Nb Process

The first RSFQ process that has been investigated during this research is an academic tri-layer process. For the study, the JeSEF (Jena Superconductor Electronics Foundry) LTS RSFQ fabrication process has been used [12]. This is the foundry being developed for European SCE activities.

The JeSEF process (see Figure 4.1) has three metal layers including the ground plane (M0, M1 and M2) using Niobium (Nb) and a Molybdenum (Mo)-resistor layer R1. To reduce the probability of pinholes in the isolation layers leading to interlayer shorts between the conducting layers, the isolation is carried out in two separate steps – one by Niobium oxide and the other by Silicon oxide. M0 and M1 are separated by I0A and I0B, while M1 and R1 are isolated by I1A and I1B. The T1 layer defines a JJ, which is a tri-layer, being a sandwich of Nb/Al-AlO_x/Nb.

The tri-layer is constructed using a single mask. It actually consists of a sandwich of 3 layers, two Nb layers acting as the electrodes with the Al_2O_3 sandwich in-between. This is done in order to minimize the formation of pinholes in the thin barrier. A cross-section of the total process is shown in Figure 4.1. The minimum dimensions for interconnection width and spacing are 5 μm. The critical current density J_c for the process is 1 kA/cm^2 and the sheet resistance of the Mo-resistor layer (R1) is 1 Ω/square. The junction capacitance for the process is 0.05 pF/μm^2.

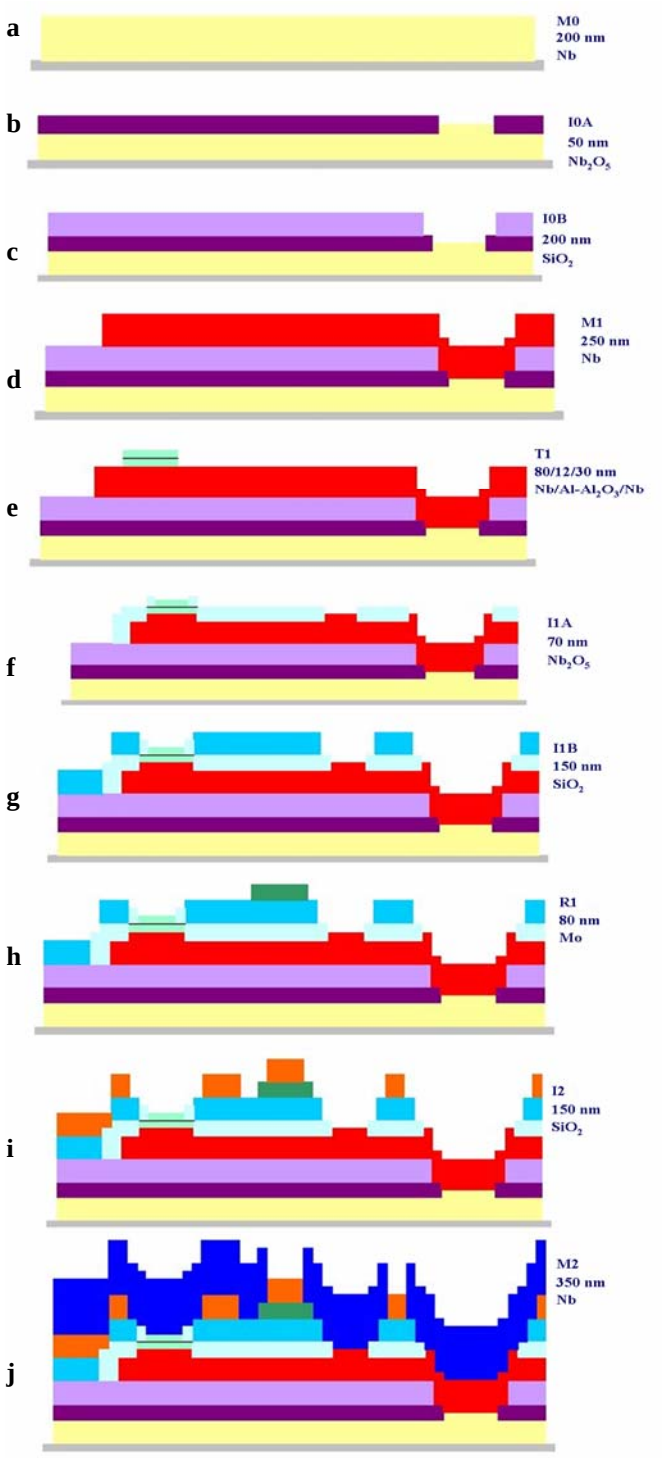


Figure 4.2: Process flow of the JeSEF Nb process.

Table 4.1: Mask Definitions of the JeSEF Process.

GDS II No.	Name	Layout polarity	Material	Thickness (nm)	Description	Mask polarity
1	M0	+ve	Nb	200	Ground plane	dark
2	I0A	-ve	Nb_2O_5	50	Holes in anodisation	dark
3	I0B	-ve	SiO_2	200	Holes in isolation	clear
4	I0C		SiO_2		Reserved	
5	M1	+ve	Nb	250	Metal Wiring1	dark
6	T1	+ve	Nb/Al/Nb	60/12/30	Tri-layer package	clear
7	I1A	-ve	Nb_2O_5	70	Holes in anodisation, Definition of junction	dark
8	CUT	+ve	---	---	Cutting of bridges for anodisation	clear
9	I1B	-ve	SiO_2	150	Holes in isolation	clear
10	R1	+ve	Mo	80	Resistance layer	clear
11	I2	-ve	SiO_2	150	Holes in isolation	clear
12	M2	+ve	Nb	350	Metal Wiring 2	dark
13	R2	+ve	Au	~40	Bond pads, optional	dark

The complete process incorporates 13 mask steps as shown in Table 4.1. The first column gives the GDS II layer (a format in which layout information is transferred). The layer name is given in the second column. The polarity of the layout layer is provided in the third column (The layout polarity is said to be positive (+ve) if the physical layer corresponding to the design drawing remains on the wafer after the process step; it is said to be negative (-ve) if the physical layer will be removed from the design area.) while the material and thickness are given in the fourth and the fifth columns respectively. The sixth column describes the layer and the polarity of the mask is given in the last column. The mask polarity is said to be clear if the photomask is transparent in the design areas corresponding to the layout and dark if it is opaque corresponding to the layout pattern. The process flow of the JeSEF Nb process is shown in Figure 4.2.

Table 4.2: Trilayer Characteristics.

No	Material	Thickness (nm)	Description
1	Nb	80	First electrode deposition
2a	Al	12	Aluminium deposition
2b	Al_2O_3	2 - 3	Oxidation of Al to form the junction barrier
3	Nb	30	Counter electrode deposition

The first step of the JeSEF process is to deposit a 200 nm Nb ground plane as shown in Figure 4.2a. Then a 50 nm Niobium oxide is formed by anodisation. This layer is grown from the Nb layers by selective anodisation. For this purpose, structures in the M0 and the M1 layers have to be connected to an M0 path for collective anodisation of the wafer. This is achieved by creating special lines for this purpose, which can be removed later on during a special mask step (CUT). Holes in the anodisation layer are implemented by the defined I0A layer as in Figure 4.2b. A 200 nm Silicon oxide is then deposited and the I0B layer definition will define the required holes in that layer (Figure 4.2c). The first wiring layer M1 of 250 nm Nb followed by the tri-layer T1, which is a sandwich of Niobium, Aluminum oxide and Niobium (Figure 4.2d and e). The characteristics of the trilayer are presented in Table 4.2. The first column gives the sub-layer number while the second column provides the material used for the implementation with its thickness in the third layer. The description of the sub-layer is given in the last column. The deposition and patterning of the other layers follows (Figure 4.2f-j). This process does not incorporate any passivation step other than the native Niobium oxide, which is a hard oxide, protecting the Niobium from further oxidation. For contact pads there is an option of using gold deposition to allow a good, low resistance contact to the pads.

4.3.1 Probable Defects in the JeSEF Process

An investigation was carried out to identify and understand the probable defects that could occur in the JeSEF process. As a first step, the design rules were checked for locating the “weak-spots” in the process. As the process was being under development, the availability of a large variety of real circuit layouts was a problem. A few cells were obtained from TU-Ilmenau, Germany via the Fluxonics network which is part of the European Society for Applied Superconductivity [13] and is working towards the initiation of the development of the JeSEF foundry. Two cells (a splitter and an SFQ-DC converter which are representative for a simple and a rather complex design) were analysed along with the design rules and 27 probable defect locations or weak-spots were identified for the process.

The details of the defect locations are presented in Table 4.3. The second column describes the defect location indicated by the serial number in the first column. An educated guess was used, based on the geometry as well as the frequency of occurrence, to compile this list of defects [14] (see chapter 3 for defect definition). The following issues are the details used for the selection of test structures for an extensive analysis of the JeSEF process later on.

Defects in the junction barrier were reported to be the most significant defect in the JeSEF process. It was reported by JeSEF staff [15] that approximately 1 in 1000 is shorted in their JJ chain for voltage standard chips, while other defects have not been shown to occur. But, this information is not final as a structural study was not yet carried out on the JeSEF process. A SEM photograph of a problem in a JJ is shown in Figure 4.3a. where misalignment of the layer I1B and I2 can be seen.

Table 4.3: List of predicted defect locations in the JeSEF Process.

No	Description of the weak-spot location
1	Bridge in the tri-layer
2	Crack in M2 above a via between M2 and M0
3	Crack in M2 above a via between M2 and M1
4	Crack in M2 above a via between M1 and M0
5	Crack in M1 at a via between M1 and M0
6	Crack in M2 above a JJ
7	Bridge between M2 and M1 next to a JJ in I1A
8	Bridge between M1 and M2 above a via between M1 and M0
9	Bridge between M2 and M1 next to a shunt or next to a JJ in I1A and I1B
10	Bridge in a shunt resistor
11	Open in a shunt resistor
12	Open in I2 above a shunt
13	Bridge between I1A and I0B
14	Short between M1 to M0
15	Bridge between M1 and M2 when they run parallel or cross each other
16	Bridge of I2 next to a shunt resistor
17	Short in M2 above a shunt resistor
18	Short in the M1 layer
19	Crack or Open in M1 when it crosses M0
20	Short in the M2 layer
21	Crack or Open in M2 when it crosses M1
22	Bridge in I1A above a via
23	Bridge in I0A above a via
24	Bridge in I1B above a via
25	Bridge in I1A above a JJ
26	Bridge in I0B above a via
27	Bridge in I2 above a via

The step coverage of a deposited layer can influence the quality of the interconnect. Bad step coverage can cause local thinning of layers, which in turn causes weak-spots prone to opens. It is known from semiconductor processing that evaporation of layers (especially Silicon oxide) can cause problems at locations with high underlying topology. From our conducted SEM analysis on some available test chips from JeSEF containing a few structures for parametric characterisation, it was clear that two locations of layer thinning are expected to be a potential problem for the top Nb layer (M2):

- Where M2 runs across a step in an underlying M1 layer
- Where M2 runs across via edges (with 150 or 200 nm step height).

The location where M2 (350 nm) crosses an edge in the underlying M1 (250 nm) is considered more sensitive to M2 defects, because it is a very severe step in the process with more than 70% of the layer thickness of M2. Our SEM analysis of this location showed that it could be problematic as seen in Figures 4.3c-d. The above situation occurs approximately twice per JJ and occurs if narrow wiring lines (< 5 μm) enter and leave the junctions.

Figure 4.3b shows a resistor contact to M2 where a probable crack can occur due to the remnants formed in the lift-off process. This is a typical problem in processes where a lift-off technique is used for patterning of layers.

The locations where metal layers step over vias are shown in Figures 4.3e-f where potential step-coverage problems can occur. The steps in M2 are explained further in Figure 4.4.

The Nb interconnect lines contain weak spots of a nature that is known to cause serious problems to integrated circuits. For the M2 wiring, it is assumed that defects at the weak spots dominate over other defects as evident from the analysis conducted on the layer [15]. Figure 4.4a shows a cross section of the expected dominant defect at the location where the M2 layer crosses an edge in the M1 layer. The layer legend is given in Figure 4.2. Figure 4.4b shows another possible weak spot in M2. This is where M2 crosses edges of holes in

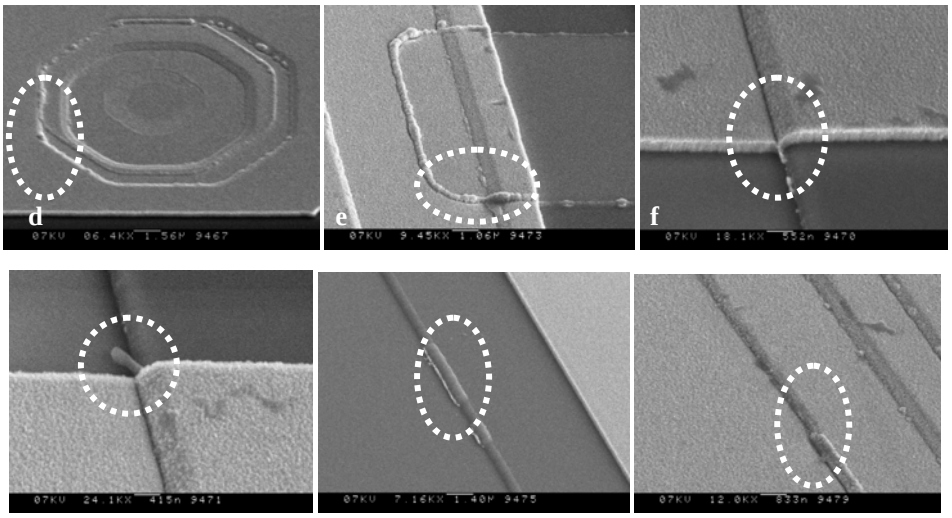


Figure 4.3: SEM analysis of a JeSEF sample chip for locating possible defect-prone locations in the process. a) a JJ, misalignment in the I1B and I2 layers is visible; b) close up of a resistor contact near a JJ showing remnants of the lift-off technique; c) Step of M2 over an M1 edge, a step coverage problem of the Si-oxide underneath the M2 Niobium is visible d) same as c but also extra material a for probable short to adjacent M2 line; e) Edge of a via from M1-M0 and f) Edge of a via from M2-M0 showing potential step-coverage problems.

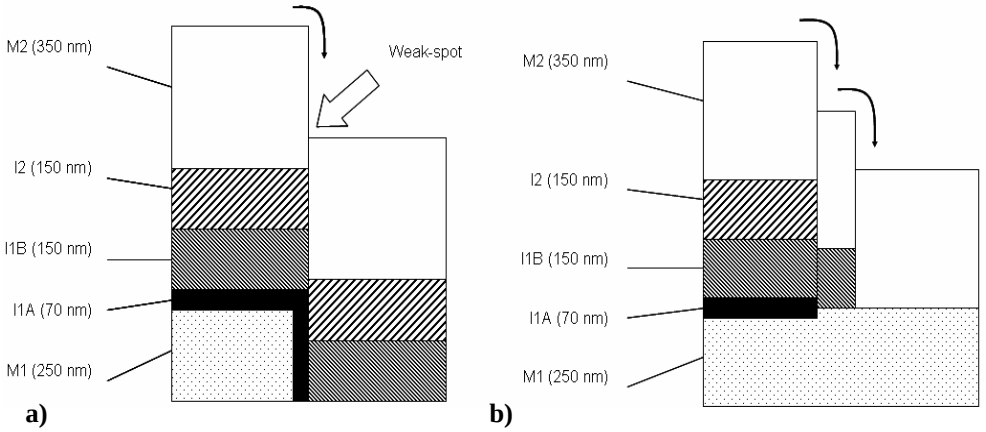


Figure 4.4: Cross-sectional examples of the M2 steps in the JeSEF process. a) step coverage of M2 at an M2-M1 Edge; b) step coverage of M2 over an M2-M1 via (see Figure 3.4 for details).

oxide layers, at vias and junctions.

Another probable defect is in the resistor layer as mentioned before. Opens and near-opens in the shunt and bias resistors are considered to be the most relevant defects concerning the resistor layer R1. A Mo resistor is likely to contain (partial) opens due to its relative thin (80 nm) nature; bias resistors are more likely to contain such defects in real circuits, since the total area of R1 is larger for these resistors. The contacts between M2 and R1 at the resistor terminals may have an open as indicated in Figure 4.3b. The leads to the resistors may also have opens in them.

Hence, the most probable defects that could occur in chips processed at the JeSEF foundry are as presented in Table 4.4. The second column lists the defects whose nature is presented in the third column. These are the locations which received major attention during this research while developing the test-structure chip for the JeSEF process. A detailed discussion of the development of the test chip is presented in the next section.

4.3.2 Structures for the Detection of Probable Defects in the JeSEF Process

The goal of the above study was to design a test chip for the JeSEF RSFQ process, that allows detection and localization of the defects listed in Table 4.4. Development of simple and easily-testable structures was crucial during the design phase. The following goals were set in designing the test structures that consist of elements of realistic circuits:

1. to obtain information on the manufacturability of complex RSFQ circuits in the process,
2. to observe the defects that actually occur in realistic circuits and
3. to determine their physical nature and to develop corresponding models for them.

From the available information, it was planned to perform dedicated, detailed tests on relevant defects that are observed in the above test chip in a next generation chip. Those detailed tests would also include tests for defect densities, defect-size distributions and critical dimensions. The present test structures were chosen such that:

a) They are representative for the elements occurring in realistic circuits processed in this foundry (e.g. obey the design rules),

b) They can reveal the expected most probable faults as predicted by the earlier study

c) They reveal information that applies to a targeted circuit complexity of 3500 Josephson junctions. (This target complexity is an estimated requirement by us for the implementation of a delta ADC with BIST).

Table 4.4: List of the most probable defect locations in the JeSEF Process.

No.	Defect Type	Nature of the defect
1.	Junction defects	Shorts and opens in metal electrodes, excessive size and number of pinholes in the thin barrier.
2.	M2 wiring layer defects	Opens or cracks (near opens) in the metal layer as a result of underlying steps in M1
3.	Resistor defects	Opens or near opens in the M2 to resistor contact, opens and near opens in the Mo resistor, shorts in the Mo layer.
4.	M2 via defects	Opens or near opens as a result of an underlying via

The purpose of the test structures is to find defects by electrical means, to locate them to a reasonable degree by electrical means and then to further investigate the defects physically. The physical analysis can be performed using known Failure Analysis (FA) techniques, such as optical microscopy, Scanning Electron Microscopy (SEM), Transmission Electron Microscopy (TEM) and Focus Ion Beam (FIB) cutting to reveal its exact cause.

The original plan was to implement all structures for Room Temperature (RT) measurements, since Low Temperature (LT) measurements consume more time than a corresponding automated RT measurement due to the additional requirement of bonding and cooling. But, there is no information available regarding the translation of defects from RT to LT. Hence, the establishment of a correlation between the two types of structures was also a primary concern.

Basically two types of structures were proposed. One set for LT, 4 K, measurements and the other set for RT, 294 K, measurements. This reduces unnecessary complexity in the testing phase and test running costs. If necessary, the LT structures can be tested at RT and vice versa. A discussion about the development of the test structures has been presented in chapter 3 of this thesis.

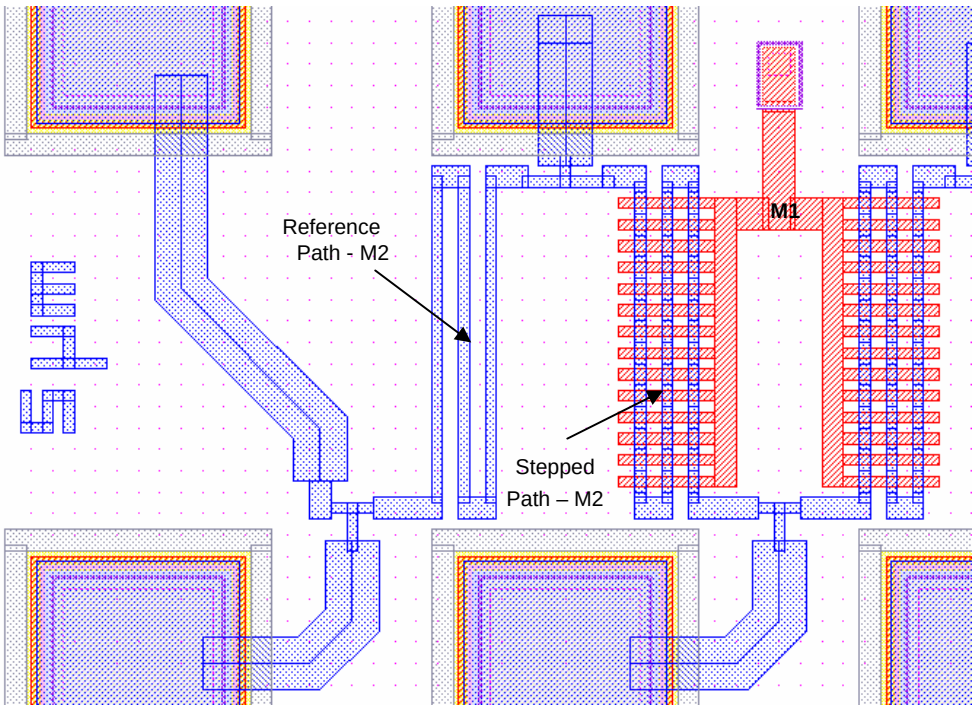


Figure 4.5: A part of the layout of the test structure to detect opens and near opens in the M2 layer over an M1 layer edge.

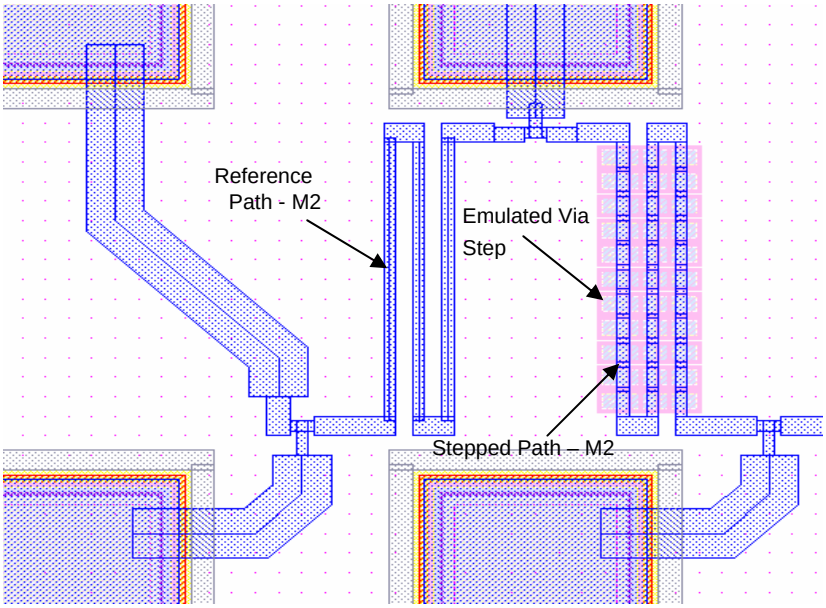


Figure 4.6: A part of the layout of the structure for the detection of defects in the M2 layer in the case of a step-coverage problem over a via.

Now, the structures for the detection of the defects mentioned in Table 4.4 will be discussed in detail. Part of the layout of the test structure to detect opens and near opens in the M2 layer if it crosses an M1 edge as is shown in Figure 4.5. The presence of a defect is detected by comparing the resistance of the reference meander to the stepped meander in the Van der Pol structure as indicated in chapter 3 of this thesis. Here, the M2 meander is laid over M1 wires to create the desired step for defect detection.

Figure 4.6 depicts the structure for the detection of defects resulting from the step-coverage problem of the M2 layer over a via to the M0 layer. The via is emulated by creating a step that is equivalent to the via step in the M2 wiring by removal of the corresponding isolation layers from below the M2 layer (see chapter 3). These structures are designed such that there is only one conducting path for the measurement current. The ratio of the resistance between the reference path and the stepped path of the above structures gives information with regard to the presence and severity of the defect in them [16].

Figure 4.7 shows various structures that have been developed for the JeSEF process. Measurement of bias and shunt resistances are carried out using structures as shown in Figure 4.7a and Figure 4.7b. A drawback of this structure is that a reference value is not attainable except from the sheet resistance structure for the Mo layer, since a reference path is not present in these structures. The reference value of the resistance has to be determined from the design value applying the measured sheet-resistance in case of variation due to allowed parametric spread in the process. The structure for the measurement of sheet resistance has been taken from [17].

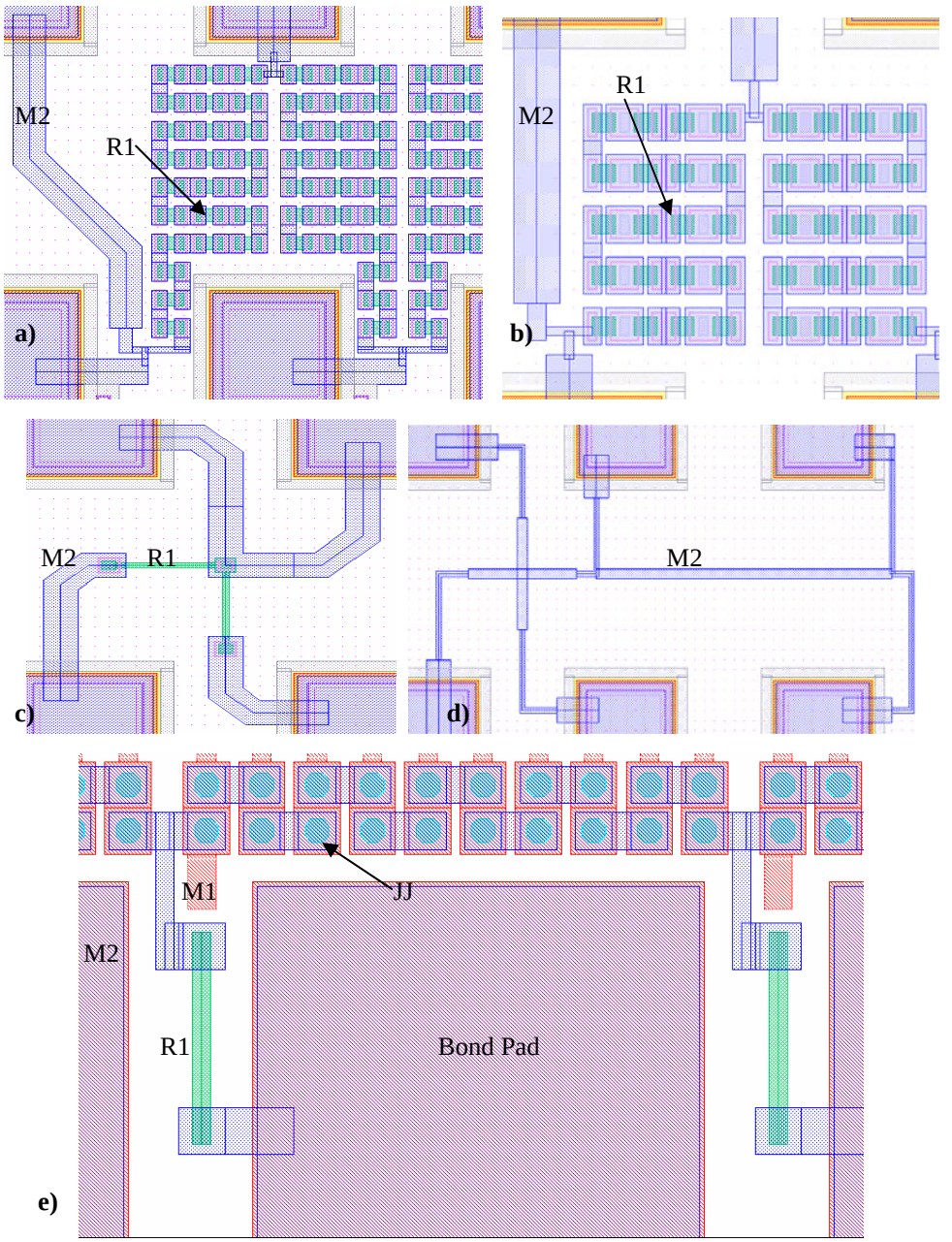


Figure 4.7: Parts of various test structures developed in the JeSEF process for the detection of defects. a) shunt-resistor chain structure; b) bias-resistor chain; c) M2-R1 contact resistance and d) M2 sheet resistance for RT measurements and e) a JJ chain for LT measurement (see chapter 3 for details).

Figure 4.7c shows the structure (Kelvin contact resistor) used to measure a contact resistance between two layers, in this case an M2-R1 contact. A sheet resistance measurement structure for the M2 layer is as depicted in Figure 4.7d. These two structures have been described in [17].

All these structures are designed to be measured at RT, using a semi-automatic probe station as it is not possible to probe at LT conditions.

The LT structure for the determination of defects and possible statistics in a JJ is shown in Figure 4.7e. A measured I-V curve of the structure will reveal any defect present in the corresponding JJ chain. The development of these structures has been presented in chapter 3 of this thesis.

4.4 The HYPRES Nb Process

The second process that was under investigation is a matured process from HYPRES, an SCE company in NY, USA [18], [19]. This is a proven and commercial process used for realising complex devices in SCE [20], [21]. The cross-section of the process is given in Figure 4.8. The standard critical current density J_c of this process is 1 kA/cm^2 for the design of RSFQ circuits. The minimum feature-size in the process is 3 μm with junction capacitances of 0.06 pF/μm^2. Higher current densities of 2.5 and 4.5 kA/cm^2 are also currently available, which will help in obtaining a higher device density per unit area. The process features four Nb metal layers labelled M0, M1, M2 and M3. The layer R3 of Ti/Pd/Au provides a low-resistance as well as contact for chip bonding.

M0 is the primary ground plane, deposited on an oxidised Silicon wafer. M3 can be used as a second ground plane to design more stable circuits (better design margins and chip-level isolation from environmental noise) or if required as a wiring layer. M1 and M2

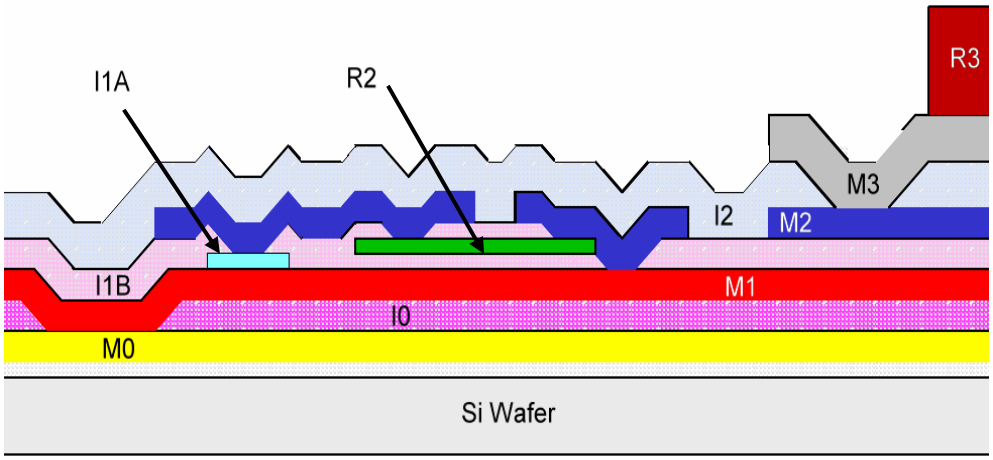


Figure 4.8: Cross section of the HYPRES Nb process.

are used as wiring layers and if a JJ is defined, they will act as its two contact electrodes. To reduce the probability of pinholes in the isolation layers leading to inter-layer shorts, the isolation is carried out in two separate oxidation steps by depositing SiO_2 using the same mask. The layers M0 and M1 are separated by I0, while M1 and R1 are separated from M2 by I1B and I2 isolates M2 from M3. The I1A layer defines a JJ, which is a tri-layer consisting of 3 sandwich layers, being two Nb layers acting as the electrodes with the Al_2O_3 in-between. As mentioned in the previous section, this is required to minimize the formation of pinholes in the thin barrier. This is achieved by depositing the entire wafer with Niobium base electrode, then by Aluminium further oxidized to Al_2O_3 and finally the Niobium counter electrode. The etching step follows patterning both the M1 wiring layer as well as the JJs.

The HYPRES process incorporates 10 masks as shown in Table 4.5. The first column

Table 4.5: Mask Definitions of the HYPRES Process.

Mask Step	GDS II No.	Name	Thickness (nm)	Material	Description	Layout /Mask Polarity
1	-	-	100	Nb	Ground plane (M0) deposition	-
	30	M0	-	-	Defines holes in the ground plane	-ve/ Dark
2	-	-	150	SiO_2	Insulation layer deposition	-
	31	I0	-	-	Via between M1 and M0	-ve/ Dark
3	-	-	135/11/45	Nb/Al/Nb	Nb/AlOx/Nb tri-layer deposition	-
	1	M1	-		Tri-layer base electrode definition	+ve/Clear
4	2	I1A	-	-	Counter electrode (JJ) definition.	+ve/Clear
5	-	-	100	SiO_2	Insulation layer deposition	-
	9	R2	100	Mo	Medium value resistor patterning	+ve/Clear
6	-	-	100	SiO_2	Insulation layer deposition	-
	3	I1B	-	-	Via between M2 and I1A, R2 and M1	-ve/ Dark
7	6	M2	300	Nb	Wiring layer 2	+ve/Clear
8	-	-	500	SiO_2	Insulation layer deposition	-
	8	I2	-	-	Via between M2 and M3	-
9	10	M3	600	Nb	Wiring layer 3	+ve/Clear
10	11	R3	350	Ti/Pd/Au	Low value resistor/contact pads	+ve/Clear

gives the mask step or level number of the process. The second column indicates the GDS II layer number of the corresponding layer in the third column. The thickness of the layer and the material used for its fabrication are given in the fourth and the fifth columns and the sixth column provides the description of the layer. The layout and mask polarities are given in the last column. These steps are carried out in 39 sub-steps as given in Table 4.6 corresponding to the process flow shown in Figure 4.9.

At first, a 200 nm Nb ground plane is deposited on an oxidized Si wafer. This is patterned using the M0 layer definition. The first isolation layer is then deposited followed by I0 patterning thereby defining the contact holes between the ground plane and the upper metal layers. The deposition of the tri-layer is carried out next. This is done by the deposition of an Nb layer of 135 nm thickness followed by an Al layer of about 6 nm and further oxidation to about 11 nm and then depositing another Nb layer of 45 nm all-in-one step. This is to guarantee a very good uniformity in the thin oxide barrier throughout the wafer (Figure 4.9a). Pattering of the M1 wiring layer and the I1A layer follows defining the first interconnect layer and the JJs. An insulation layer of 100 nm of SiO_2 followed by the medium-value Mo resistor layer (1.0 Ω/□) R2 of 100 nm and another isolation of 100 nm (Figure 4.9b). The I1B pattering step follows which defines all vias between the M2 upper layer to the resistor layer R2, junction counter-electrode I1A and the wiring layer M1. Further, a 300 nm of Nb is deposited. The M2 wiring layer is patterned followed by the fourth isolation layer using 500 nm of SiO_2 (Figure 4.9c). Next, the I2 patterning follows which defines a via between the wiring layers M2 and M3. Deposition of the third wiring layer M3 and patterning as well as the deposition of the low-value resistor layer (0.05 Ω/□) R3 follows (Figure 4.9d).

The next section deals with the investigation into the probable locations of weak spots in the process.

Table 4.6: Sub-steps in the HYPRES Nb Process.

Part 1: (Figure 4.9a)	**Part 2: (Figure 4.9b)**	**Part 3: (Figure 4.9c)**	**Part 4: (Figure 4.9d)**
1. M0 Deposition	10. M1 Photoresist	22. I1B Photoresist	30. I2 Photoresist
2. M0 Photoresist	11. M1 Etch	23. I1B Etch	31. I2 Etch
3. M0 Etch	12. Resist Strip	24. Resist Strip	32. Resist Strip
4. Resist Strip	13. I1A Photoresist	25. M2 Deposition	33. M3 Deposition
5. SiO_2 Deposition	14. I1A Etch	26. M2 Photoresist	34. M3 Photoresist
6. I0 Photoresist	15. Resist Strip	27. M2 Etch	35. M3 Etch
7. I0 Etch	16. SiO_2 Deposition	28. Resist Strip	36. Resist Strip
8. Resist Strip	17. R2 Deposition	29. SiO_2 Deposition	37. R3 Evaporation
9. Tri-layer Deposition	18. R2 Photoresist		38. R3 Photoresist
	19. R2 Etch		39. R3 Etch
	20. Resist Strip		
	21. SiO_2 Deposition		

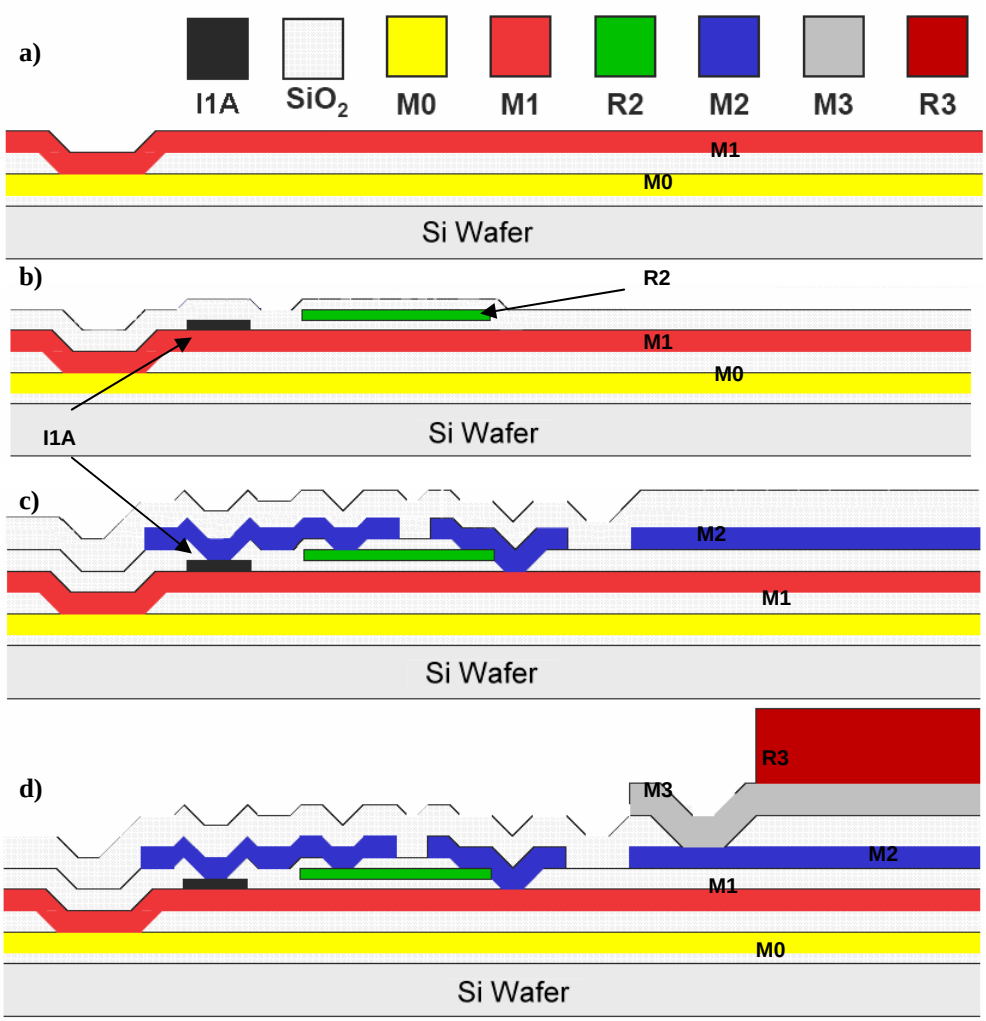


Figure 4.9: Process flow of the HYPRES Nb process.

4.4.1 Probable Defects in the HYPRES Process

Before discussing the probable defects in the HYPRES process, it is worthwhile to mention the remarkable (structural) differences from the JeSEF process. The major ones are relating to the number of metal layers, junction geometry and definition, structuring of layers and methodology for isolation. The JeSEF process features three metal layers while the HYPRES process offers four with the possibility of an additional ground plane or wiring layer. JeSEF uses an octagonal junction and anodisation of the Nb layer while HYPRES employs square JJs and SNEP (Selective Niobium Etching Process). For structuring of the layers, JeSEF uses a lift-off technique while HYPRES uses an etching process. While the etching allows for better step coverage for layers, the drawback is “bias effect”. The bias effect is the phenomenon by which the size of the structure on the wafer maybe different from the design layout characterised by the so-called bias. Bias is defined as the difference of the linear size (linewidth) of a structure on the wafer and the design linewidth. JeSEF uses two separate masks for the isolation while HYPRES isolates the layers by two separate steps in the deposition.

The above mentioned differences affect the occurrence of probable defects in the HYPRES process as compared to the JeSEF process. Due to the increase in the number of metal layers, the probability of additional defects between the layers also increases. The bias effects increase the probability of an open or a crack due to thinning of the wiring layer. Furthermore, contrary to the report from JeSEF [15], it was stated that junction defects are not common in the HYPRES process apart from parametric defects (e.g. variations in J_c). Evaluating these facts and comparing the information from semiconductor industry, it was concluded that the majority of the structural defects in the HYPRES process arise from interconnects. Hence, specific care was given to interconnect wiring while investigating the weak-spots in the process.

As previously in the case of the JeSEF process, an investigation was carried out to determine the defect-prone locations in the HYPRES process. A study of the design rules for the process was the first step in this investigation. This study revealed 31 possible locations in which a defect can occur due to the topography of that particular location (or weak spots). A limited number of test structures were available at HYPRES to detect inter-layer shorts using long meander structures apart from those used for parametric tests and were evaluated. These structures had drawbacks such that only the presence of a short can be detected but localization of the defect is not possible and the presence of intra-layer opens will result in a wrong conclusion. New structures were designed (using the information available from the previous study on JeSEF) and incorporated into two of the test chips available before starting a detailed investigation of the process. A SEM analysis was carried out on those chips. Some of the detected defect-prone locations are shown in Figure 4.10. As mentioned before, bias effects seem to affect the process severely as seen in Figure 4.10a and c. Figure 4.10a shows the extreme results of the bias effect which is an open in the wiring layer: the wire under the dotted line is etched away. Another class of defects (manufacturing defect) which has been observed is mechanical damage from dicing as seen in Figure 4.10b. Figure 4.10d shows presence of an extra M3 material causing an intra-layer short in the M2 layer. Apart from this, mask misalignments also cause an

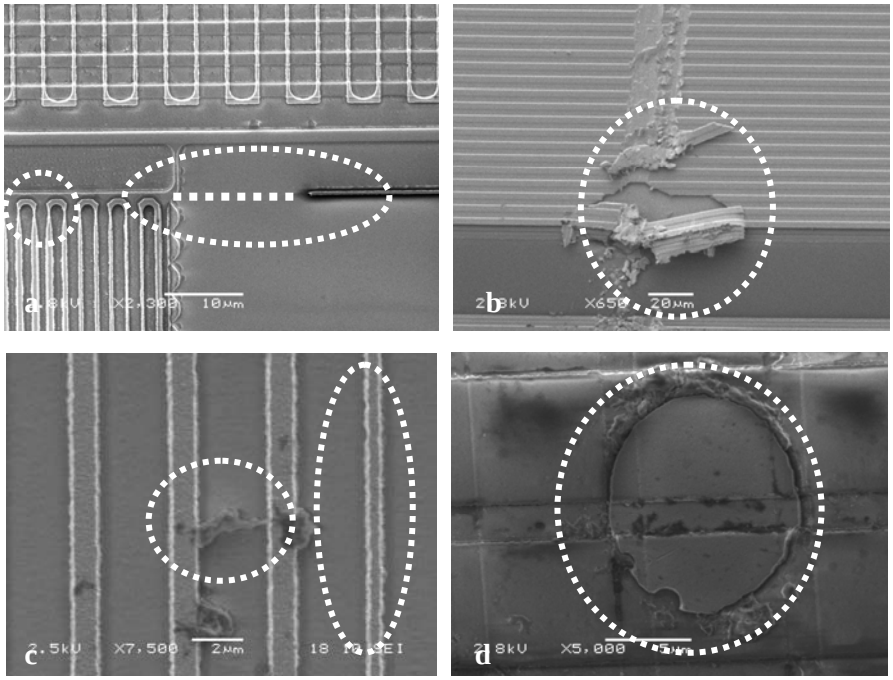


Figure 4.10: SEM analysis carried out on an available HYPRES sample chip for locating possible defect-prone locations in the process. a) open in the wiring layer M3 and near-opens due to bias effects; b) mechanical damage occurred on the M2 layer during dicing of the chip; c) an intralayer short of the M3 wiring layer due to extra material and a bias effect resulting in the thinning of M3 wire and d) an extra material (M3) causing a short to the adjacent line in M2.

Table 4.7: List of predicted defect locations in the HYPRES process.

No	Description of the weak-spot location
1	Crack / open in M3 above a via between M3 and M0
2	Crack / open in M3 above a via between M3 and M1
3	Crack / open in M3 above a via between M3 and M2
4	Crack / open in M2 above a via between M2 and M0
5	Crack / open in M2 above a via between M2 and M1
6	Crack / open in M2 above a via between M1 and M0
7	Crack / open in M1 at a via between M1 and M0
8	Crack / open in M2 above a JJ
9	Short between M3 and M2 over an edge in the M2 layer
10	Short between M3 and M2 over an edge in the M2 and M1 layers
11	Short between M2 and R2 over an R2 edge
12	Short between M2 and M1 next to a JJ in I1B
13	Short between M1 and M2 above a via between M1 and M0
14	Short between M2 and M1 next to a shunt resistor
15	Bridge in the tri-layer
16	Bridge in a shunt resistor
17	Open in a shunt resistor
18	Open in I2 above shunt resistor leading to an intralayer short in M2
19	Bridge between M1 and M0 over an edge in an underlying layer
20	Bridge between M1 and M2, when they run parallel or cross each other
21	Bridge of I2 next to a shunt
22	Bridge in M2 above a shunt
23	Short in the M1 layer
24	Open in the M1 layer
25	Short in the M2 layer
26	Open in the M2 layer
27	Short in the M3 layer
28	Open in the M3 layer
29	Bridge in I0 above a via
30	Bridge in I1B above a via
31	Bridge in I2 above a via

increase in the probability of the defects: for instance, contact masks shifted in the opposite direction for an M1-M3 minimum size via results in a defective contact hole. Even though it is possible to detect misalignment by other means, it is not the main purpose of the structure. It should be noted that development of an automated in-line defectivity measurement is desirable before commercialising the technology.

The initial list of probable defects is shown in Table 4.7. The second column provides the description of the defect. This information was used for the second step in the investigation – analyzing the predicted locations in real circuits. Since the HYPRES process is an established one, various cell libraries were available for analysis. Two cell

libraries (a part of them) designed in the process were used in this stage for the investigation. The first one was cells obtained from HYPRES Inc [22] and the second one was from Chalmers University, Sweden [23]. The predicted locations resulting from the above study as given in Table 4.7 were crosschecked with the two obtained cell libraries.

Examples of the cross-sectional analysis of the cells are shown in Figure 4.11. The HYPRES cells are shown in Figure 4.11a and the Chalmers cells are shown in Figure 4.11b. The following cells have been analysed: DC-SFQ and SFQ-DC converters, Splitter, JTLs, D-Type Flip Flop, T-Type Flip Flop, Merger and standard interconnections for joining cells together. About 25 locations in the HYPRES cells as well as 20 locations in the Chalmers cells as shown in Figure 4.11 showed the predicted interlayer weak-spots. The analysed locations are shown as numbers over the cells (Figure 4.11).

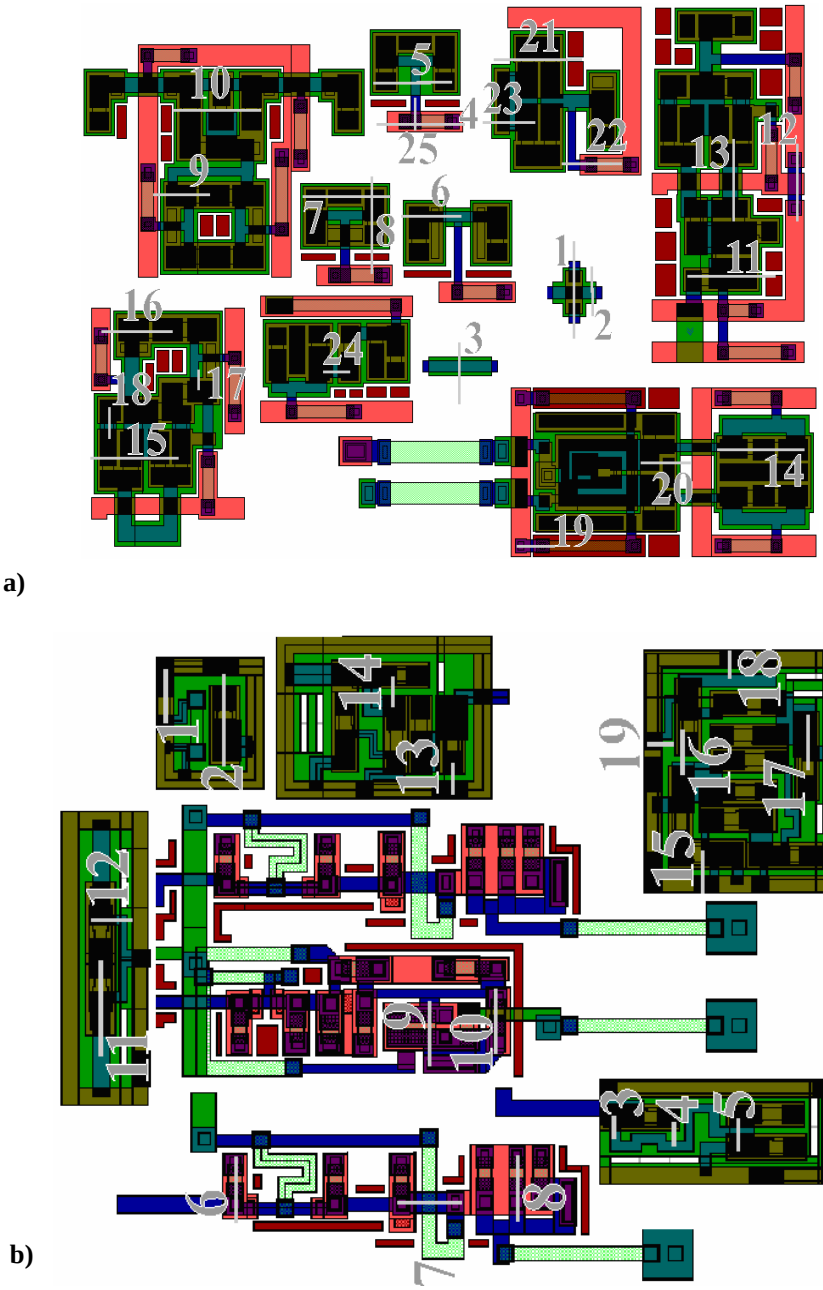
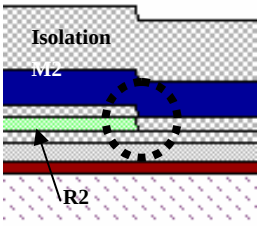
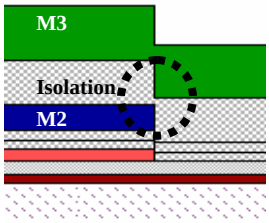
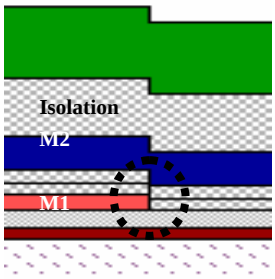


Figure 4.11: Library cells designed in the HYPRES process showing the interlayer weak-spot locations. a) cells obtained from HYPRES Inc; b) cells obtained from Chalmers University (see text).

A brief summary of severe interlayer shorts is given in Table 4.8. The defect type is given in the second column with the corresponding cross-sectional view in the third

Table 4.8: Examples of cross-sectional analysis on the HYPRES cell libraries.

No	Defect Type	Cross-Section	Cause of the defect	Example (see Figure 4.11)	Functional Behaviour
1	Bridge between M2 and R2 if M2 crosses R2		The isolation layer has the same thickness as R2.	HLC: 25 CLC: 7	Short in resistors
2	M3-M2 bridge if M3 crosses an edge with M2 and M1		In worst case, the isolation thickness between M3 and M2 can be 5nm.	CLC: 13, 14, 15, 18, 19	M2 is grounded, short in resistors
3	M2-M1 bridge if M2 crosses M1		In worst case, the isolation thickness between M1 and M2 can be 35nm.	HLC: 6, 12, 14, 15, 17, 18, 22, 23, 24 CLC: 3, 4, 5, 8, 9, 12, 16	Short in JJ terminals, M2 shorted to the bias line

column. The fourth column explains the cause of the particular defect and detected examples of the corresponding defect types in the layout are enumerated in the fifth column (cross-reference numbers relate to Figure 4.11). The notation “HLC” refers to the HYPRES library cells and “CLC” relates to the Chalmers library cells. The sixth column shows the resulting defective situation (functional behaviour) in the circuit. The most serious weak spot that was observed is the crossing of M2 over R2 edges leading to M2-R2 interlayer shorts. This situation arises due to the fact that the isolation layer between the M2 and the R2 layers is of the same thickness as R2 (see Table 4.5).

The next severe weak spot was found to be the crossing of the M3 layer over an edge of both M2 and M1 layers. At this location, the isolation-layer thickness between the M3 and M2 layers in the worst-case situation (considering the allowed parametric change in the thickness of layers) will be just 5 nm. Hence, the probability of the occurrence of a defect at this location is very high. Since layer M3 is being used as a second ground plane for better stability, there is a high probability of getting M2 wiring shorted to ground.

Another location is the crossing of the M2 wiring layer over an M1 edge. In worst case, the isolation thickness will be about 35 nm. This case occurs very often at a JJ and the resulting situation shorts the terminals of the JJ. The M1 layer is also extensively used for supplying bias currents to the JJs, hence there is also a probability of shorting an M2 wiring with the bias lines. Apart from this, several possibilities of cracking, opens or near-opens, in the top metal layer over a via interconnect were also investigated.

To summarise, firstly the probabilities of weak spots based on processing steps were investigated. Then, to determine the possibility in real circuits, the corresponding cell library was examined. The resulting information was used for the development of test structures. The details of various structures developed for the evaluation of process are presented in the following section.

4.4.2 New Test Structures for the HYPRES Process

As mentioned before, the HYPRES process was said to be a matured commercial process and hence it was assumed during the development phase of the test structures that the parametric variations would be less influential in this process. Furthermore, due to the structural differences in the investigated processes, the probabilities of different defects can be different in both. Finally, due to the high cost for realisation, only a limited number of chips could be placed per wafer and hence the gathered information was bound to be limited. The increase in the number of interconnects creates defects of more complexity to occur in the process than the earlier study. It was decided that all possible interconnect defects have to be investigated for the HYPRES process in order to extract as much information as possible about the predicted defects.

The above arguments give rise to the following consequence: more structures have to be designed and tested in a small available area and still be representative for the realistic defects in the process. Hence, the number of the same type of structures was reduced and more structures of different types were substituted. The major outcome of this is that a wafer mapping, as explained in chapter 3, cannot be carried out as in the case of the JeSEF process since the available data is not sufficient from the limited number of structures per chip. But since parametric deviations were not the primary concern, as well as the availability of the parametric test structures at HYPRES in case it is required, made this action justifiable. Furthermore, the number of JJ structures was also reduced according to the information received from the foundry itself. Junction defects (apart from parametric deviation) were not observed in the HYPRES process while using their own test chip. The number of resistance structures were also considerably reduced in the HYPRES design as it was clear from the earlier study on the JeSEF process that the probability of structural defects in them is much lower than the parametric defects. Experimental results are presented in chapter 5 of this thesis to support this argument.

As the first step, the structures that have been designed earlier for the JeSEF process were translated into the HYPRES process [24], [25]. Some adaptations were made to the structure as it was observed that the irregularity in the structure caused by the reference structure at the beginning of a chain is affecting the measurements and corrections had to

be applied in the case of previous designs. This is due to the fact that the resistance differs for the first lead of the structure (see for e.g. Figure 4.6) and a real 4-point measurement cannot be carried out at the edges of the structures due to the additional lead resistances induced by the irregularity. This was corrected by placing the reference path on the second segment of the chain as shown in Figure 4.12. In the case of a via structure, since the etching process is used at HYPRES, a metal layer is required as etch-stop under the isolation layer. Hence the design of the structure, to avoid occurrence of a second defect or allowing a second conducting path, was more challenging than the JeSEF case. The adapted structure is shown in Figure 4.13 for the detection of a crack of M2 over an M2-M1 via. The M1 layer was spread as a mosaic pattern and the via structure was placed over it with the M2 wiring. The second type of a via problem associated with the contact-hole was addressed in a different structure by connecting a series of minimum-size vias in a chain as depicted in Figure 4.14a. A four-point measurement scheme can be implemented by using the four terminals of the structure.

Other new structures were also developed, as the HYPRES process is matured and the investigation was extended to all possible interconnection wires. Two examples of structures are given in Figure 4.14b and Figure 4.14c.

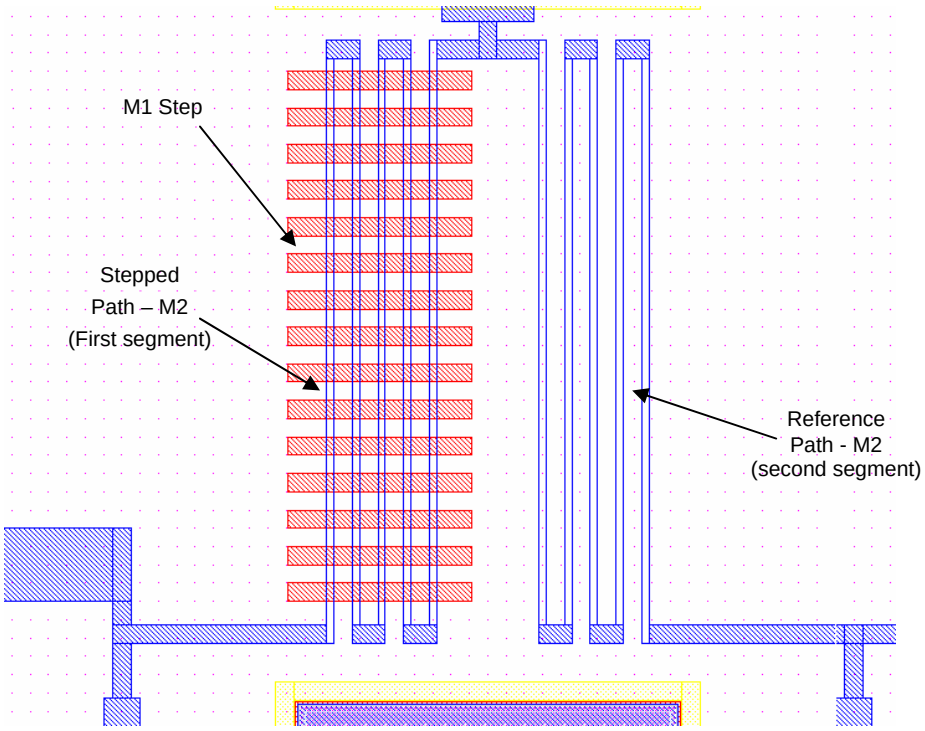


Figure 4.12: A part of the layout of the adapted test structure to detect opens and near opens in the M2 layer over an M1 layer edge. (See Figure 4.5 for comparison).

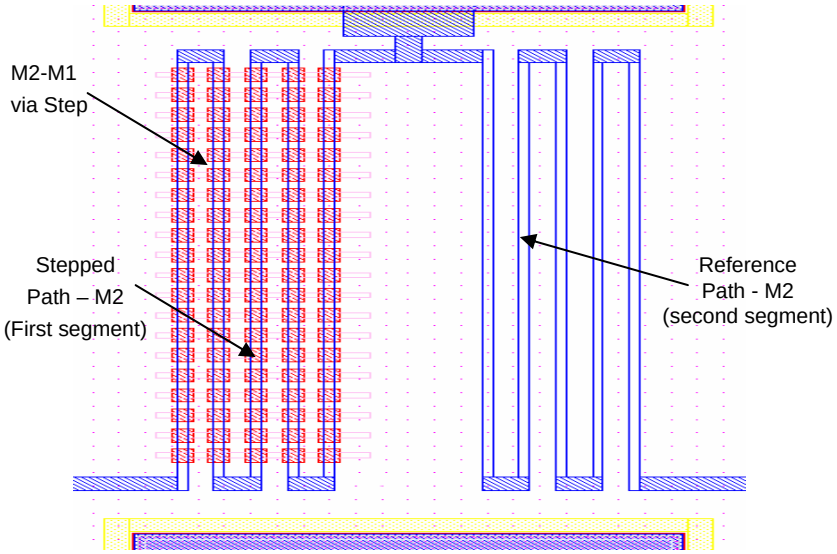


Figure 4.13: A part of the layout of the adapted test structure to detect opens and near opens in the M2 layer over an M2-M1 via. (See Figure 4.6 for comparison).

Figure 4.14b shows a comb-meander structure designed to detect the intra-layer short in the M1 layer. This structure is an interleave of a meander with two comb structures as described in chapter 3 of this thesis. The terminals T1, T7 and T4, T6 are the two ends of the meander and the combs are connected to T2, T3 and T5, T8 respectively. The double connection is inserted to facilitate four-point measurements on the structure. The continuity of the meander is first measured by applying a four-point measurement on T1, T4 and T6, T7 as the current and voltage pair respectively. A short is detected if the measurement between any of the T1/T7 with T2/T3 or T5/T8 results in a measurable resistance.

The second example given in Figure 4.14c is that of a structure for the detection of interlayer shorts between the M2 and R2 layers. A short is detected by a measurable resistance between the terminal (T1) of the big top meander and the bottom meanders T2, T3, etc. (see details in chapter 3).

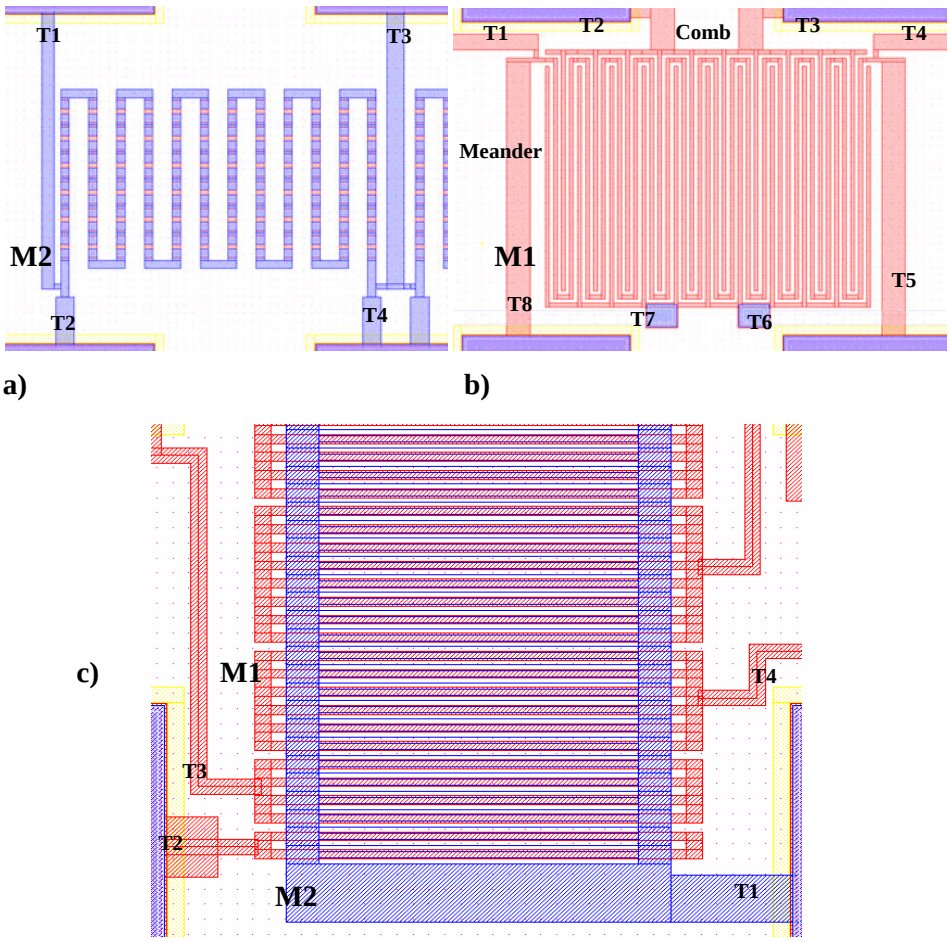


Figure 4.14: Parts of structures developed for the HYPRES Nb process: a) a chain via structure for detecting contact-hole problems in the M2-M1 via; b) a comb-meander structure to detect intralayer shorts in the M1 layer and c) special meanders for the detection of interlayer shorts between M2 and M1 over an M1 edge (see Chapter 3).

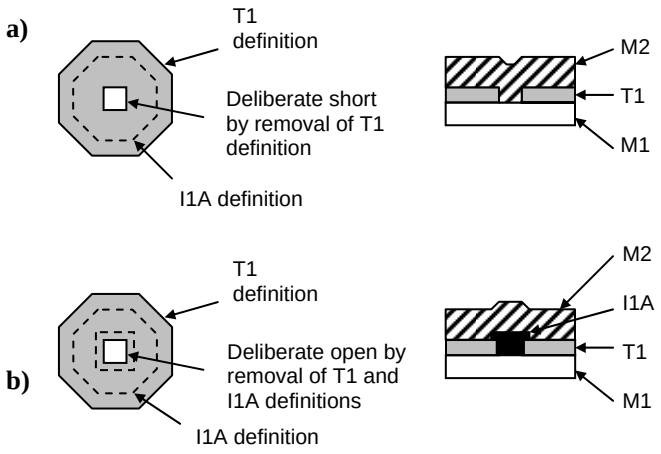


Figure 4.15: Insertion of deliberate defects into a JJ designed in the JeSEF process and corresponding cross-sectional view. a) a short in the tri-layer (T1); b) an open in the tri-layer (T1).

4.5 Special Test Structures for Junction Measurements

As mentioned in chapter 3 of this thesis, the detection of probable defects in a JJ has to be carried out at 4.2 K using a structure, (as shown in Figure 4.7e), designed to reveal the most important junction quality parameters such as V_m (a measure for the junction leakage) and the critical current of the unshunted junction [26], [27]. The method consists of an IV-curve measurement of several long series of JJs. From the IV-curves it can be determined whether one of the long series possibly contains a defective JJ. A long series of JJs that is suspected to contain a defect can be further investigated in detail by performing IV-curve measurements on segments of the long series. The procedure can be repeated down to segments containing 20 JJs in series as in Figure 4.7e which can be further analysed optically if required.

The disadvantage with this method is that bonding is required for the JJ access pads to the circuit board for measurements for each time-consuming thermal cycle, since there are only a limited number of signal lines available in a cryo-probe. This limits the number of measurements that can be carried out per cycle, again depending on the number of signal lines in the used cryo-probe. An alternative LT access technique using a Be-Cu fingerboard design [28] for the JJ structures restricts the number of structures that could be placed with reasonable localization of the defect. Hence a balance should be established on the basis of the results after preliminary experiments on the structures.

Furthermore, to study the effects of defects in a JJ at low temperature, it was required to conduct real experiments on a defective junction. For this purpose, two of the defects that are most probable in a JJ were deliberately inserted into the layout to create defective junctions. The results will be used to verify the proposed fault-models for a JJ. The

insertion of defects is implemented as shown in Figure 4.15. The details of the insertion of a short in a JJ in the JeSEF process is given in Figure 4.15a. The tri-layer T1 is partially removed thereby creating a short between the M2 and M1 layers inside a JJ. This can be considered as a large pinhole in the tri-layer. Figure 4.15b shows the details of the insertion of a deliberate open. Here, both the T1 and I1A definitions are removed so that the hole is filled by the isolation material SiO_2.

As mentioned in the third chapter of this thesis, the idea to carry out all measurements at room temperature is our final goal as this will reduce the test time and costs enormously. The main idea was to establish a correlation between the 4.2 K and 294 K measurements. Several approaches were considered for this purpose. One approach is to create a capacitor structure using a JJ. Since a JJ consists basically of two metal conductors separated by a non-conducting interface at room temperature, this can be considered to be a capacitor in a broad sense. The practical problem is to get reliable results from a capacitor structure while measuring extremely small values in the range of a few hundreds of femto Farad for an actual JJ.

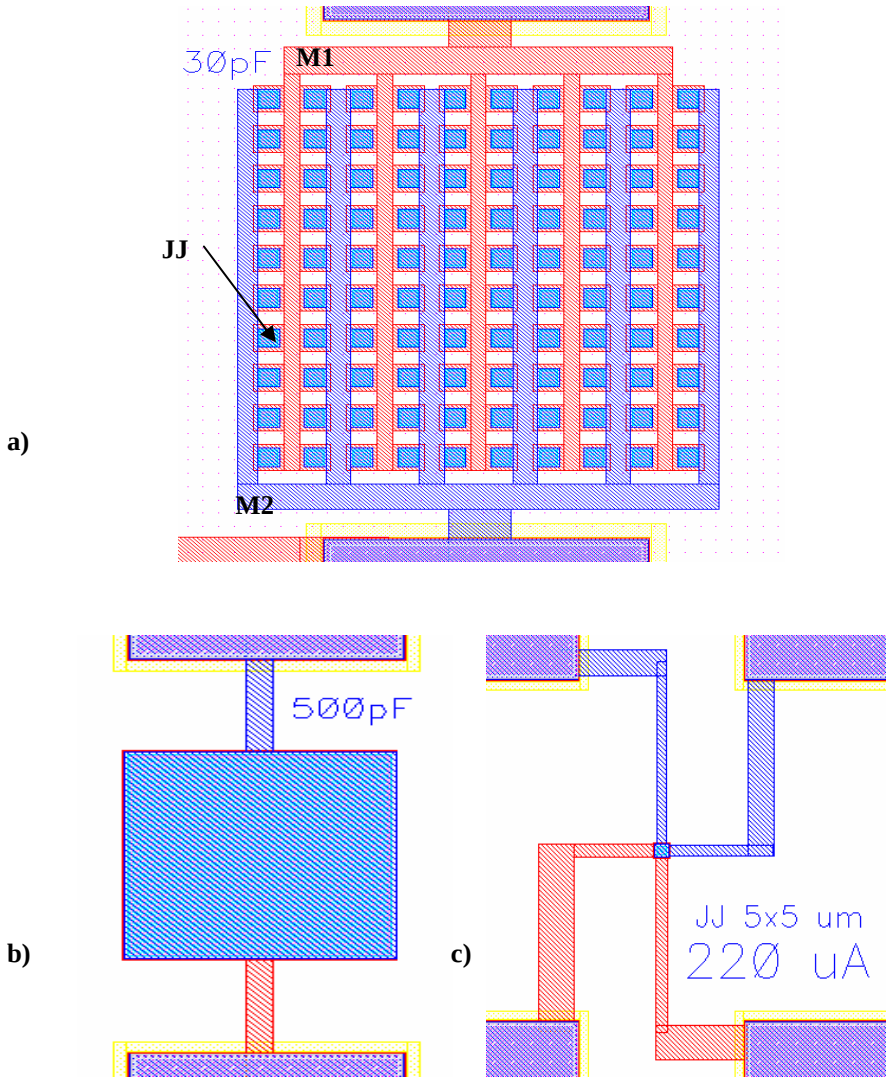


Figure 4.16: Special room-temperature structures for the detection of defects in a JJ: a) a parallel capacitor structure; b) a large capacitor structure and c) a contact structure to determine the junction resistance.

A number of JJs were connected in parallel to overcome this problem thereby increasing the measurable capacitance of the structure as shown in Figure 4.16a. Large area JJs were also implemented for this purpose as depicted in Figure 4.16b. The disadvantage of these structures is that they are not representative for a real JJ. The accuracy of the measurement required to detect a change in the capacitance due to a single defective JJ is yet to be determined by real experiments using deliberatively defective JJs. Another approach is to measure the contact resistance of a JJ and relate it to the low temperature characteristics [29], [30]. The corresponding test structure is shown in Figure 4.16c.

4.6 The Implementation of Test Chips for Defect Data

The implementation of the suggested structures in test chips was the next task. As mentioned in the previous sections, a balance is required to extract useful measurement results from the test structures. The initial test chips designed by us for the HYPRES process were very simple. One of the examples is as shown in Figure 4.17. It consists of meanders for intralayer shorts and opens, interlayer shorts, metal step-coverage problems, and the scaling of the layers. In order to extract information on the probability of defects, special care has to be taken with regard to the implementation. The number of structures required in a test chip as well as the grouping of the test structures are important factors in the implementation.

It should be ensured that no more than one defect is detected at a time in a group of structures. Furthermore, the detected defect has to be localised electrically to a reasonable degree of resolution in order to allow further physical investigation (e.g. by SEM) of the defect. Measures should be taken so that the statistical variations on the electrical parameters of the test structure do not obscure the presence of a defect. Keeping in mind the available information in the semiconductor industry [31], test structures for structural defects have to satisfy the requirement that the structure should be able to detect yields in the range of 20 to 80%. This requirement sets limits to:

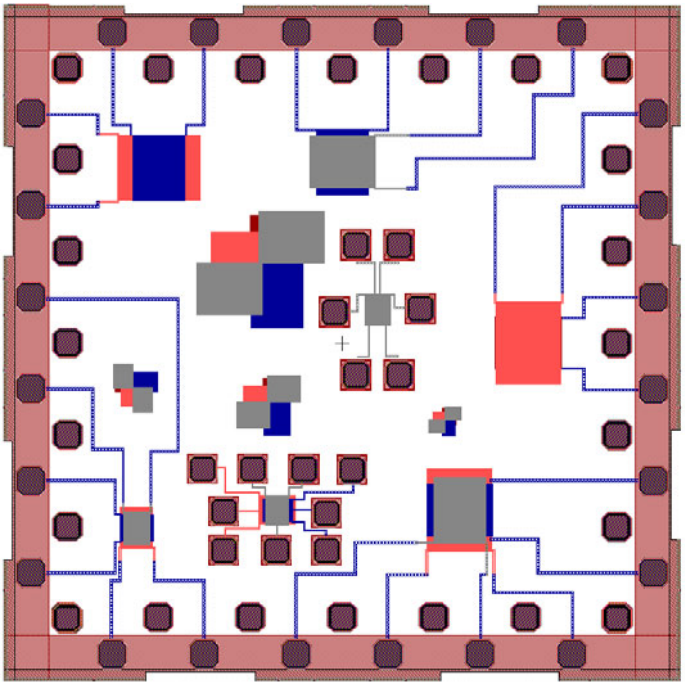


Figure 4.17: One of the preliminary test chips (HYPRES_June02) designed for investigating the HYPRES Nb process consisting of structures for intralayer shorts and opens, interlayer shorts, metal step-coverage problems, and scaling of the layers (isolated structures) for optical inspection.

1. the minimum number of structures that is required to make sure to find at least one defect in the case of a yield of 80%,

2. the maximum number of structures that is allowed to be tested at once, to make sure that no more than one defect is found in the case of a yield of 20%.

As a result of the first requirement, the number of structures to be tested should be 20 times the expected occurrence of the same structural situation on a chip of the target complexity set. On the assumption that defects in the structures under test occur independently and with a probability '*p*', and '*N*' is the number of structures under test as it occurs on the chip of the required target complexity, the smallest probability that has to be detected for the 80% yield requirement is p_{min} given by [31]:

$$0.80 = (1 - p_{\min})^N \rightarrow 1 - p_{\min} = \sqrt[N]{0.80} \qquad (4.1)$$

In order to have 99% confidence that at least one defect is found, the number '*M*' of objects under test implemented in the test structure has to satisfy:

$$1 - (1 - p_{\min})^M = 1 - 0.80^{\frac{M}{N}} \geq 0.99 \rightarrow \frac{M}{N} \geq 20.6 \qquad (4.2)$$

Hence, in order to satisfy the second condition i.e. to be 99% sure that no more than one defect is detected at a time in case of 20% yield, the number of objects under test in a segment M_s should satisfy the condition:

$$M_s \cdot 0.20^{\frac{M_s - 1}{N}} + (1 - M_s) \cdot 0.20^{\frac{M_s}{N}} \geq 0.99 \qquad (4.3)$$

Eqn. (4.3) gives the probability of having one defect in the segment. As an example, the M2 over M1 edges occurs twice every junction and consequently 7000 times for a chip with 3500 JJs complexity. According to (4.2) the required number of steps that should be implemented to have 99 % confidence to find at least one defect is at least 144,200 steps in case of 80% yield. Using (4.3) it has been determined that the number of M2-M1 steps should be less than 355 steps per segment (meander). It is possible to predict the required chip area, in terms of standard test grids, as a function of the number of steps per segment. By this requirement a lower limit is put on the number of steps per meander (once the available space is known). The number of occupied standard grids N_{grids}, can easily be determined by using:

$$N_{grids} = \frac{N_{total}}{N \cdot 15} \qquad (4.4)$$

where N_{total} is the total number of required steps and N is the number of steps per meander. Note that the number of stepped meanders in one grid is 15 (called the test object: explained later in the text), plus one reference meander. This forms the basis of the chosen approach for implementing the test chips. The choice of implementing the test structures as

realistic circuit elements will result in test structures that are able to detect defects relevant to realistic circuits. However, further physical investigation is required to determine the nature of the defect (e.g. exact position and size). This is a consequence of the applied method as explained above, which focuses on detection and localization of the defect.

Physical investigation of detected defects is a tedious and expensive task and there is a possibility that the actually identification can be extremely difficult because of location or small size. Moreover, marginality with respect to the test parameter will create extra work. This is because a large parametric deviation indicating a possible defect is not necessarily due to the presence of a structural defect. On the other hand marginality may also cause some defects to go undetected.

For an actual implementation, the test chips can be designed as a mixed-test purpose chip: use the same chip in which both the room and low temperature structures are placed. Or design a dedicated purpose chip, in which only one type of structures (e.g. RT) are placed. A mixed chip was preferred because of the following arguments:

- The chosen method for interfacing the junction series by bonding, only allows the junction series to be positioned near the chip edges. This results in a large unused space at the center of every chip that would be dedicated to junction defects in case standard fab sizes are used for the chips.
- In the case of a mixed RT/LT chip, the design becomes simpler since only one chip has to be designed; also the area can be used in a more flexible way.
- In case of dedicated chips for each structure, the total available area for the different types of structures should be flexible to design such dedicated chip for each kind of structures. Since different structures require different chip area, a large number of small chips are required to distribute the chip area between the different chips and this is not a favourable situation for the design.

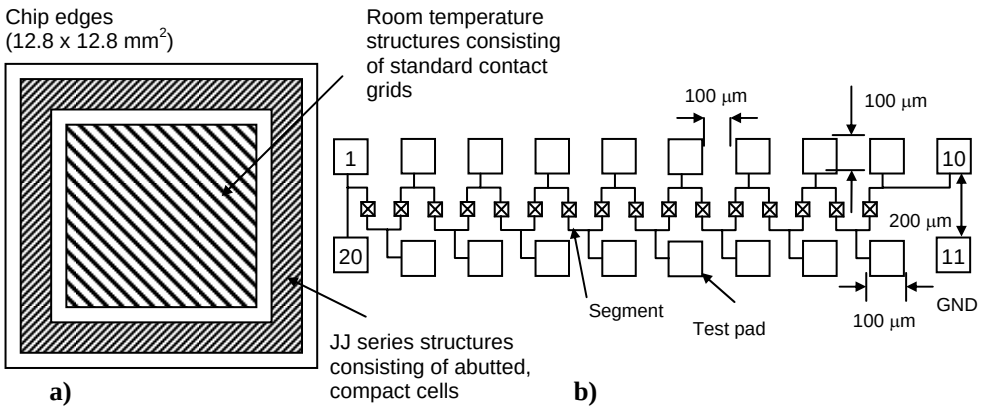


Figure 4.18: a) Floor planning for the JeSEF test chips (JeSEF_Jan02) and b) A grid of test structures showing the test pads and segments of test structures.

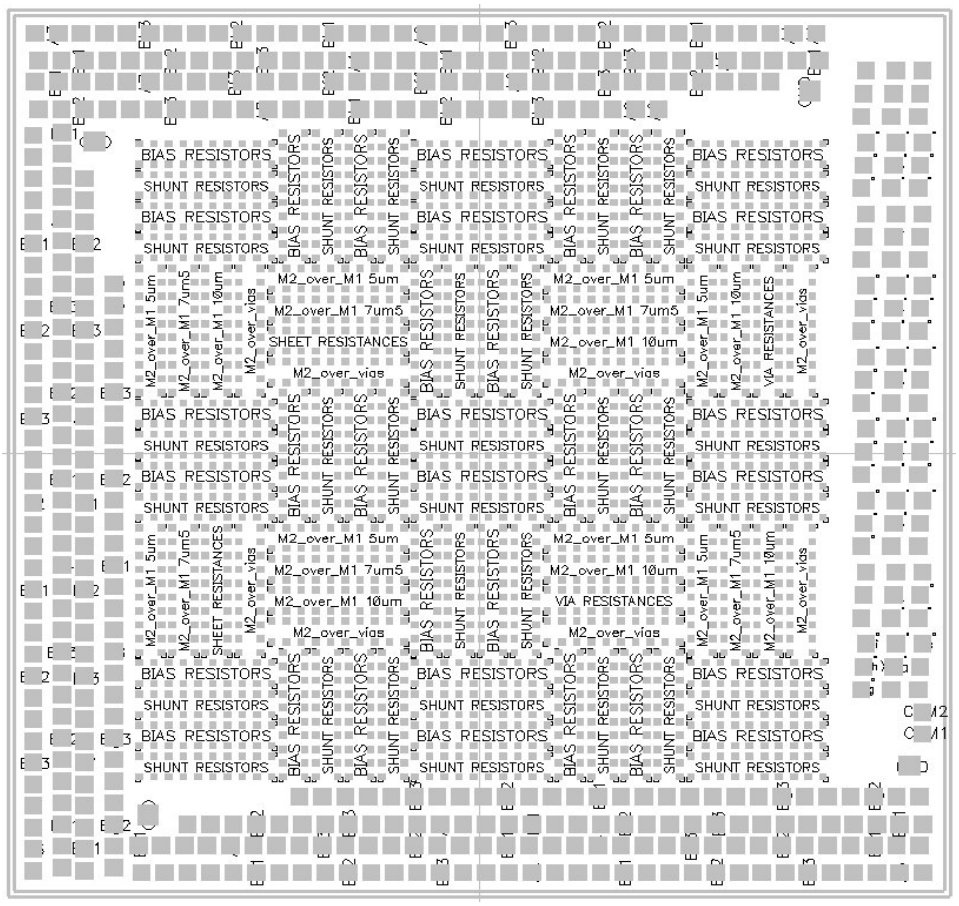


Figure 4.19: Details of the JeSEF test chip (JeSEF_Jan02) with locations of the various structures.

The LT test structures were placed at the edge of the chip and the remaining area at the center of the chip was subsequently distributed amongst the RT test structures. The floor planning for the JeSEF chip is shown in Figure 4.18a. The test chip contains three structures at the top, left and bottom edges of the chip, which each contain 2,560 JJs in series. The JJ area has been varied among the three structures to determine possible area dependencies. The critical currents of the JJs in the structures are 100 μA, 200 μA and 300 μA respectively. The fourth structure at the right contains JJ chains in which the deliberate defects as mentioned in the previous section were inserted.

In the remaining centre space, 100 standard contact grids of room temperature structures were placed in two directions (horizontal and vertical) to study the directional dependency, if there is any as the process is under development, of defect mechanisms involved. Figure 4.18b shows the contact grid for the room temperature structures. In order to achieve the number of implemented test objects that are as close to the target complexity number as possible, following Eqn. (4.4), the RT structures have been implemented as

densely packed structures. This is however resulting in a compromise of the measurability of small defects to a certain extend as explained before. A detailed view of the JeSEF test chip is as shown in Figure 4.19.

For the implementation of the HYPRES test chip (HYPRES_Nov03), the same grid as in the case of the JeSEF test chip was used for the RT test structures. The modifications as mentioned in the section 4.4.2 regarding the HYPRES test-structure development were also implemented. The floor plan of the resulting chip is shown in Figure 4.20. The chip measures 10.3 x 10.3 mm^2 and is equivalent to 4 standard HYPRES chip sizes (5.15 x 5.15 mm^2). The structures are organized inside a 2 x 10 test pad grid as in the case of JeSEF which is suitable for our semi-automatic probe station. A total of 100 test grids are used. They are organized in 5 columns and 20 rows. In total, 38 different test structures for measurement at room temperature and 19 different test structures for measurement at low temperature have been designed and incorporated on the chip. The LT test structures were placed at the two edges of the chip as shown in Figure 4.20. Among the 100 sets of RT test structures, almost all structures are placed three times evenly distributed in the chip area. That will also allow repeated measurements and test for homogeneity within the chip area. Details of the conducted tests and results are presented in the next chapter of this thesis.

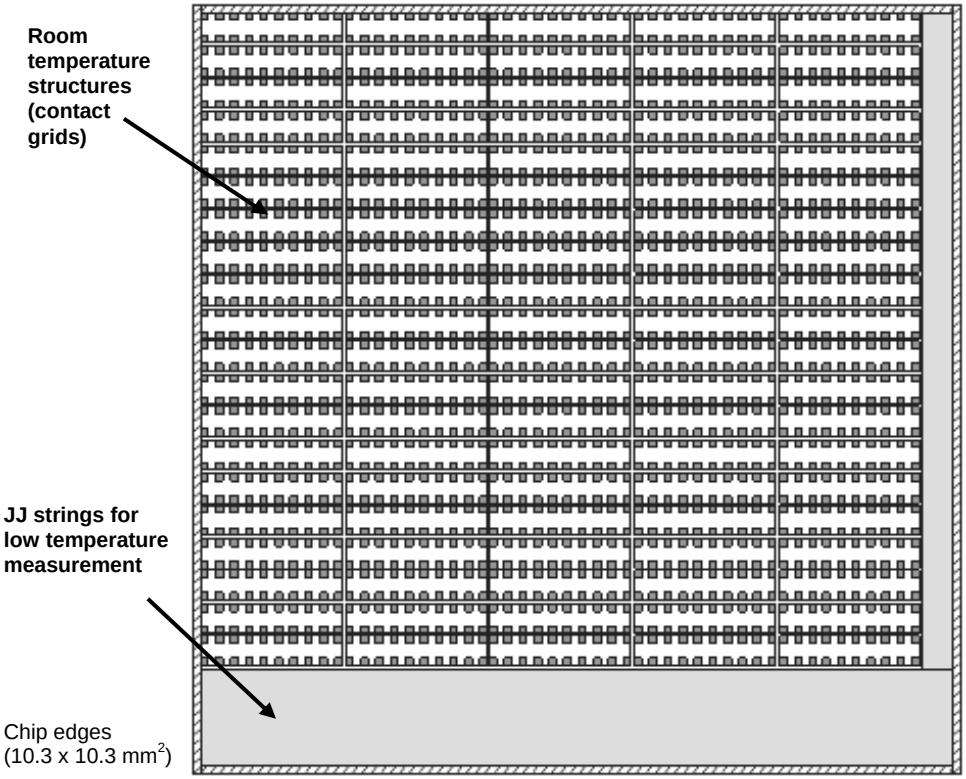


Figure 4.20: Floor plan of the HYPRES test chip (HYPRES_Nov03).

Table 4.9: Classification of defects in an LTS RSFQ Process.

Group	Defect type	Nature of the defect
1	Junction defects	Shorts, opens or excessive size and number of pin holes in the thin dielectric barrier
2	Metal-layer defects	Opens or near opens due to thinning, bridges or shorts due to excessive material
3	Resistor-layer defects	Opens or near opens in the metal-to-resistor contact, opens and near opens in the thin Mo resistor layer, bridges or shorts between resistor terminals
4	Isolation-layer defects	Opens or near opens resulting in interlayer bridges, contact hole problems in via hole

4.7 Classification of Defects in an LTS RSFQ Process

The number of predicted defects as mentioned in sections 4.3.1 and 4.4.1 does not reflect information about the quality of the process, but are predicted according to the topography of the process.

These defects can be grouped into a list of probable defect locations for the classification of defects in an RSFQ process as shown in Table 4.9. The second column states the type of defect and the third column describes the nature of the defect. The defects in a JJ are related to its thin dielectric-barrier. Shorts, opens and pinholes are believed to cause junctions to malfunction. Opens and near opens in metal layers form another class of defects, resulting from the step-coverage profile of the underlying layers. Via contact defects due to isolation problems and resistor-layer problems are other probable defect classes. This classification is an immediate result of the conducted study.

4.8 Conclusions

In this chapter, detailed investigations on two LTS RSFQ processes (JeSEF and HYPRES) have been presented. Design rules, layouts and real chips were investigated to identify potential weak spots in the process. The investigations resulted in a list of probable defect locations in the processes. Associated test structures were developed as part of the investigation. These structures are capable of detecting and localizing the relevant defects.

The first process that was investigated is an academic process, the JeSEF Nb process from Jena, Germany. A list of 27 probable defects was identified in this process. Since, the process was under development, eight test structures, including the ones capable of detecting the four types of defects which were suspected to be the most probable ones were the main focus while investigating this process. Test structures have also been developed for the JJs to be measured at low temperatures. The measurements on these structures will reveal the real nature of the defects and their statistics at LT conditions. These test

structures were incorporated into a new test chip, the JeSEF_Jan02 design. Ten identical test chips were placed per wafer on a 6” wafer containing 32 chips. This will also allow limited wafer mapping of the defects under study.

The second process that was under investigation is the HYPRES Nb process from New York, USA. This is a matured commercial process having some structural differences from the JeSEF process. In this case, a list of 31 probable defects was identified for this process. A much detailed analysis was carried out on this process since more circuits (cell libraries) were developed and available in this process. The knowledge gained from the previous JeSEF investigation was useful at this stage. Detection of defects in all possible interconnects were the primary concern as the HYPRES process was a more mature process in which parametric variations are stated to be of less concern. Thirty-eight test structures were developed for the RT measurements. Nineteen different structures were designed for LT measurements including defect-induced JJs. Three identical test chips (design HYPRES_Nov03) were incorporated per wafer on a 6” wafer containing 200+ chips. This limits the information that can be gathered by the chips from the wafer.

4.9 References

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Chapter 5

Structural Testing: Defect Analysis of the Investigated RSFQ Processes

This chapter deals with the experimental analysis of the test chips developed for the structural testing of RSFQ processes. The two processes described in the previous chapter which were investigated during this research work have been analysed. Structural test methodologies for the detection of defects are also presented. Implementation of the test routines for semi-automatic testing of the processed chips for structural defects at room temperature was carried out. The test data was analysed to provide defect statistics in both processes. This chapter presents the defect ranking of the processes leading to the most probable defects in the processes. Test methodologies for low temperature measurements are also presented and it will be proven that our approach is able to detect defects in JJs.

5.1 Introduction

Processing technologies for the realisation of RSFQ circuits were discussed in the previous chapter. Probable defects in two of the investigated processes as well as the test structures required to detect the presence of particular defects were also introduced. In this chapter, the test methodologies applied to those test structures and corresponding measurement results are presented. Four-point measurement schemes as presented in chapter 3 are implemented using a semi-automatic probe station for data acquisition.

Parametric defects are those defects by which a portion of the wafer is defective due to the fact that the electrical parameters in that region deviate beyond the allowed margins of the designed values. Or in other words it is a deviation that is measured beyond the tolerance limit. A parametrically good chip is defined as one in which these defects are absent. Structural defects or spot defects are resulting from discontinuous distributions of physical parameters (e.g. layer thickness) over a wafer. They are also called random defects due to the fact that they occur randomly over the wafer area.

The organisation of this chapter is as follows. Section 5.2 deals with the measurement methodologies involved at room temperature. Measurement analysis of the test structures in the JeSEF process is presented in Section 5.3, followed by the HYPRES process in Section 5.4. The low temperature measurement technique is presented in Section 5.5.

5.2 Measurement Techniques at Room Temperature (RT)

As mentioned in Chapter 3 of this thesis, tests for detecting defects are performed by measuring an electrical parameter (e.g. resistance) of the test structure under consideration. Deviations from a nominal parameter value are then indicative for the presence of a defect. However, the test parameter will have a certain natural variation inherent in the process. This is often assumed to be a normal distribution. The range of natural variation is a function of the number of test objects in a segment as explained in the previous chapter.

The presence of defects will cause parameter changes that result in a different distribution for the parameter values. In the ideal case, the distributions of the parameter for the defect and defect-free situation are separate. But, in a real case, there is a possibility of an overlap of the distribution by which the presence of a defect will be obscured by the natural parameter variations (in case of a marginal parameter change). A defect causing a change ΔX_{defect} will result in a shifted distribution depicted in Figure 5.1, but can be handled by careful design of the structures as presented in the previous chapters. A detailed study on this subject was presented in [1].

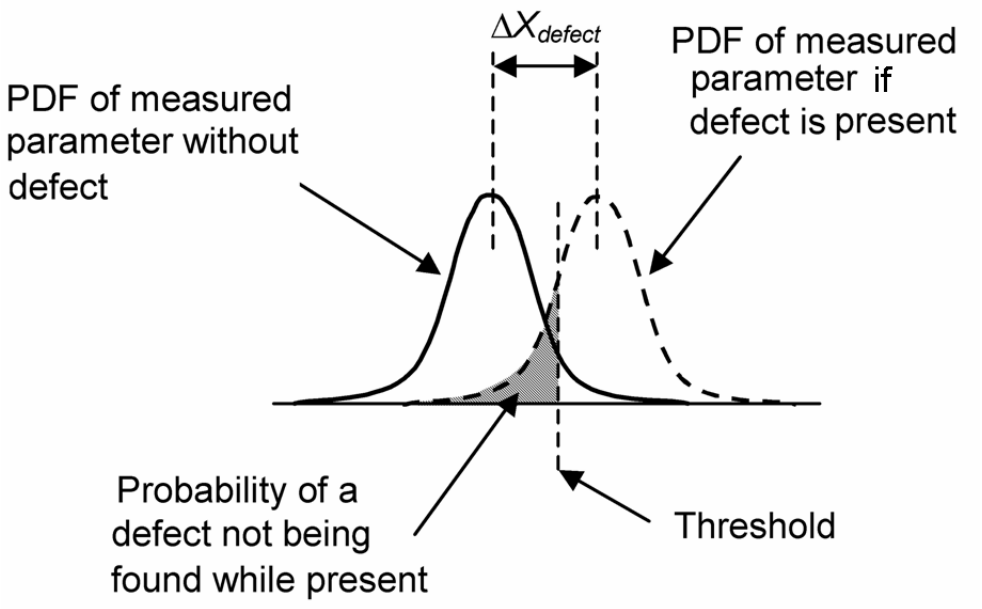

Figure 5.1: Realistic probability distribution function (PDF) of a measured parameter, if a defect is absent and present, showing possible overlap.

All RT measurements have been conducted on an Electroglas 2001X semi-automatic probe station [2]. This measurement set-up is positioned in a light-tight box. The X2001 probe station has a 6" hot-chuck and a temperature controller Temptronic TP315 [3] is available in the set-up. The TP315 has a temperature range of 0°C-200°C with resolution of 0.1°C. A 2 x 10 probe card has been used for measurements. It was first manually positioned to the reference structure of the first chip to be tested on the wafer. After positioning, a program called Integrated Circuit Measurement System (ICMS) controls the automatic measurement [4]. ICMS controls the positioning of the probe on the die as well as the type of test to be performed depending on the specific test structure.

The electrical measurements have been performed using an HP4141B Modular DC Source/Monitor and an HP3456A 6½ digit Digital Voltmeter. In combination with an HP4084B Switching Matrix Controller, the corresponding structure to be tested was selected. ICMS determines how the connections are made to different test structures via the switching matrix connected to the probe card. The four-point measurement schemes of the test structures were implemented in ICMS. Measurements were carried out by injecting a fixed current into the structures. Depending on the sheet resistance of the material (e.g. Nb) and length of the wire, the expected resistance value has been calculated. Based on the symmetry of the test structures, each measurement results in the same resistance with an allowed parametric deviation (tolerance). A large deviation of the measured value outside the tolerance limit from the expected value indicates the presence of a defect. The details of the measurement results are presented in the following sections.

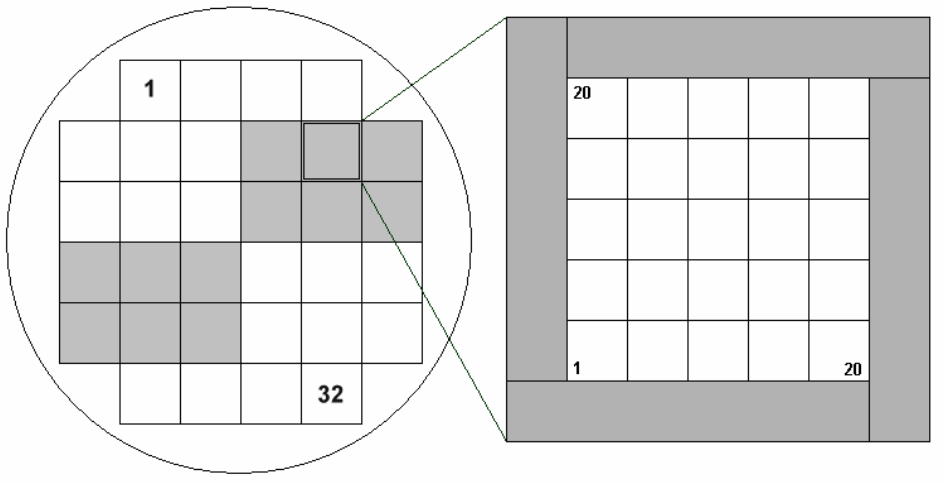

Figure 5.2: a) Diagram of a 6" SCE wafer showing the contours of test chips. The shaded ones represent our test chips to study structural defects. b) The outline of a chip showing the arrangement of RT (blank) and LT (shaded) test structures.

The raw test data produced by ICMS has been sorted using a UNIX shell script and is further analysed using MATLAB [5]. The shell script separates data from the raw output file and groups them into similar ones according to the type of the measured test structure. The MATLAB m-files written for data analysis handle the data and perform statistical calculations to identify the detected defects. It should be noted that the obtained statistics is limited due to the small number of available test ships. The data has also been graphically analysed using the Origin Graphics package [6] for data analysis.

5.3 Analysis of the JeSEF Process

Our designed test chip (JeSEF_Jan02) was processed at JeSEF (details of the design are referred to Chapter 4 of this thesis). Figure 5.2 shows the overview of the 6" wafer and the test chip. There are 32 standard slots of 12.8 x 12.8 mm^2 available on the wafer. Twelve test chips were placed in a wafer. In Figure 5.2a, the shaded portion shows the position of our test chips and the rest of the wafer was used by other customers of JeSEF. In the test chip, the location of the test structures was divided into 5 blocks of 4 test-structure grids (as mentioned in Chapter 4 of this thesis: see Figure 4.18), each as shown in Figure 5.2b. In total, there are 25 blocks of test structures or 100 grids in each test-chip. The test time for a single test chip is about 50 minutes.

For the detection of shorts, opens or near opens, the ratio of resistance of a plain meander to that of the stepped meander can be used to compare any difference showing the presence of a defect. The idea of the test structures proposed in [7] called "van der Pol" structures have been implemented for this purpose as described in Chapter 3 and Chapter 4 of this thesis.

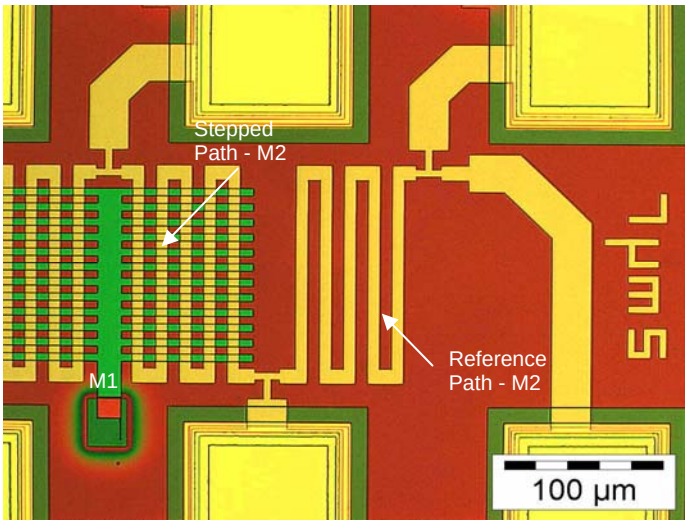

Figure 5.3: Photomicrograph of the test structure for detecting a crack in an M2 layer using a v/d Pol structure.

An example of such a processed structure is shown in Figure 5.3. This structure is designed to detect probable cracking defects in the wiring layer M2 when it crosses over layer M1. Details of the various developed structures were presented in chapter 3 of this thesis. The defect analysis of the process is complex due to the fact that the following (parametric) variations are very frequently observed in the JeSEF chips:

- Intrachip variations of parameters
- Interchip (Intrawafer) variations of parameters
- Interwafer variations

To get an idea of the extent of the above parametric variations, contour and surface plots were used. In a surface plot, the surface is plotted with two explanatory interval variables in the plotting model. It is a continuous surface of the predicted responses from the fitted parametric model on a set of regular grids of the explanatory variables. The contour plot is an alternative to a 3-D surface plot. A contour plot is a graphical technique for representing a 3-dimensional surface by plotting constant z slices, called contours, on a 2-dimensional format. That is, given a value for z, lines are drawn for connecting the (x,y) coordinates where that z value occurs. The contour plot is formed by the independent variables on the vertical (y) and horizontal (x) axes. The lines then will form the iso-response values. The independent variables are usually restricted to a regular grid. If the data (or function) do not form a regular grid, one typically needs to perform a 2-D interpolation to form a regular grid. For the contour and surface plots, the grid explained before and shown in Figure 5.2b has been used.

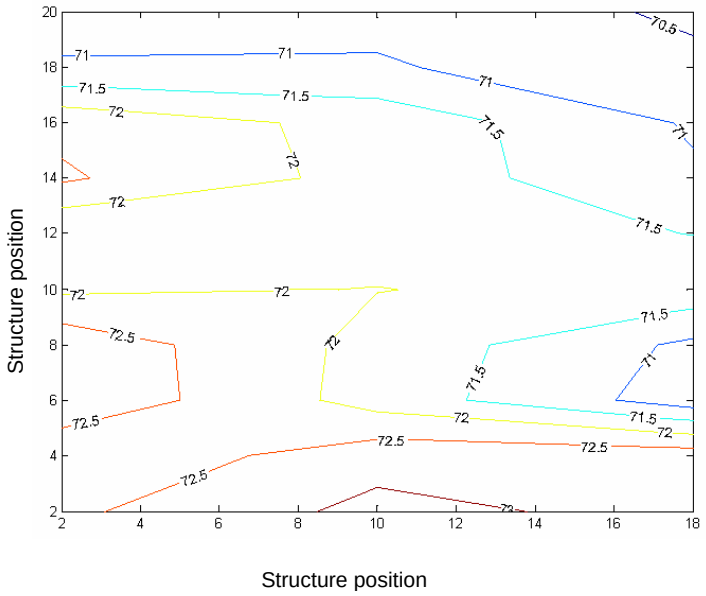

Figure 5.4: Contour plot showing the measured parametric variation of the bias resistance over a test chip JeSEF_Jan02 (the numbers on the axis refers to the position of the structure in the grid and the resistance values along the contours).

As the detected defect can be influenced by parametric variations, the chips were first analysed to find the range of process variations. This was carried out using an algorithm for statistical analysis. It was found that the variation can be as high as 70% in worst-case situations with a nominal variation of about 4% in good cases. Contour plots and surface plots were made for mapping the parameter under consideration over the chip for a better

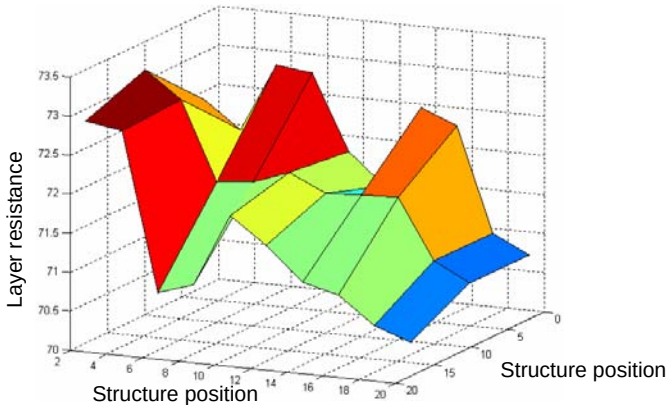

Figure 5.5: Surface plot showing the measured parametric variation of the bias resistance over a test chip (values on the x and y axis refers to the position of the structure in the grid and the resistance values are along the z axis).

understanding of the prevailing condition (these plots give a graphical representation of the parametric variation). In Figure 5.4, the contour plot and in Figure 5.5 the surface plot of the bias resistance is shown to illustrate the parametric variation in a good chip. From Figure 5.4, it can be seen that the resistance is decreasing towards the top right corner of the chip and the variation is diagonally along the chip as seen in Figure 5.5.

The following method was used for defect analysis. First, the parametric variation was determined and a "local" average value (explained later) was given to the parameter under study. This local value can be considered to be the value in the contour plot at a particular location as shown in Figure 5.4. Then the allowed process variation was compared to this value. The test structures whose parametric values are outside the limits of this allowed variation are defined to be defective. Since the parametric variations are ruled out, the resulting defect is said to be a random structural defect. The flow chart of the algorithm used to implement the analysis is given in Figure 5.6.

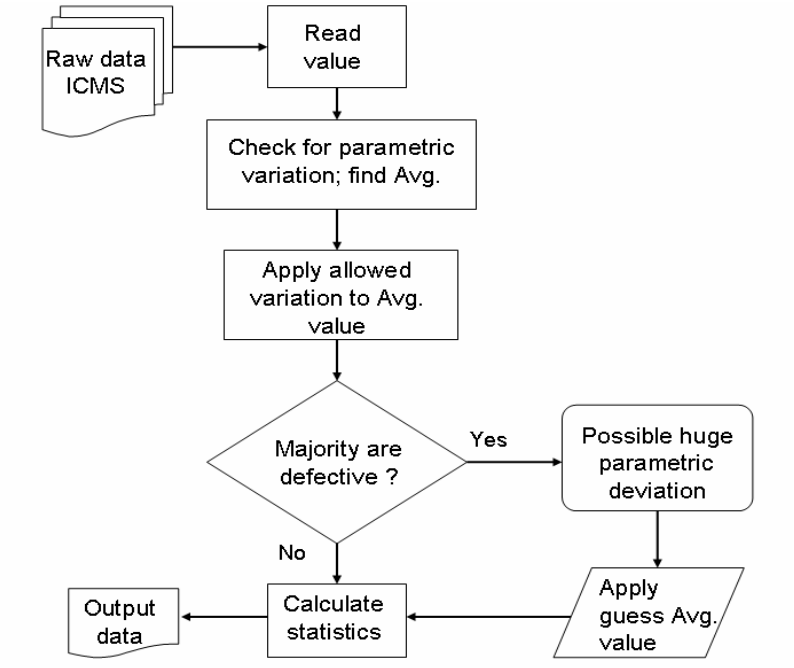

Figure 5.6: Flow chart of the implemented algorithm in MATLAB for defect analysis.

The procedure for finding the average local value is by taking the average of a row and a column of data from the input file. The input file for this calculation is the resulting output of the shell script as mentioned in Section 5.2. It contains the measured values of the test structure. There is a probability that the particular row or column has severely suffered parametric variation or a structural defect is present and has an incorrect average value. In this case, the algorithm verifies a different row/ column. But there is a probability that no suitable row/ column can be found in which no defect is present making all average values

high above the limits. In such a case, the average value has to be given manually (the value is determined by making use of the contour plot mentioned before and the graphical analysis described in the next sub-section) to determine the statistics as shown by the alternative branch of the algorithm. This algorithm was implemented in MATLAB.

5.3.1 Graphical Analysis of Defect Data

As mentioned before, the data is visualised using the Origin Graphics package. This type of representation gives a better understanding with regard to the defect to perform a statistical analysis. The analysis clearly showed that the structures were able to detect the defects, as well as indicating a clear distinction between parametric and structural defects.

Figure 5.7 shows an example of a plot where the structure grid has suffered a number of parametric defects. The presented results are from the structure which was designed to detect the step-coverage problem of the M2 wiring over an M1 edge (JeSEF wafer # 1176,

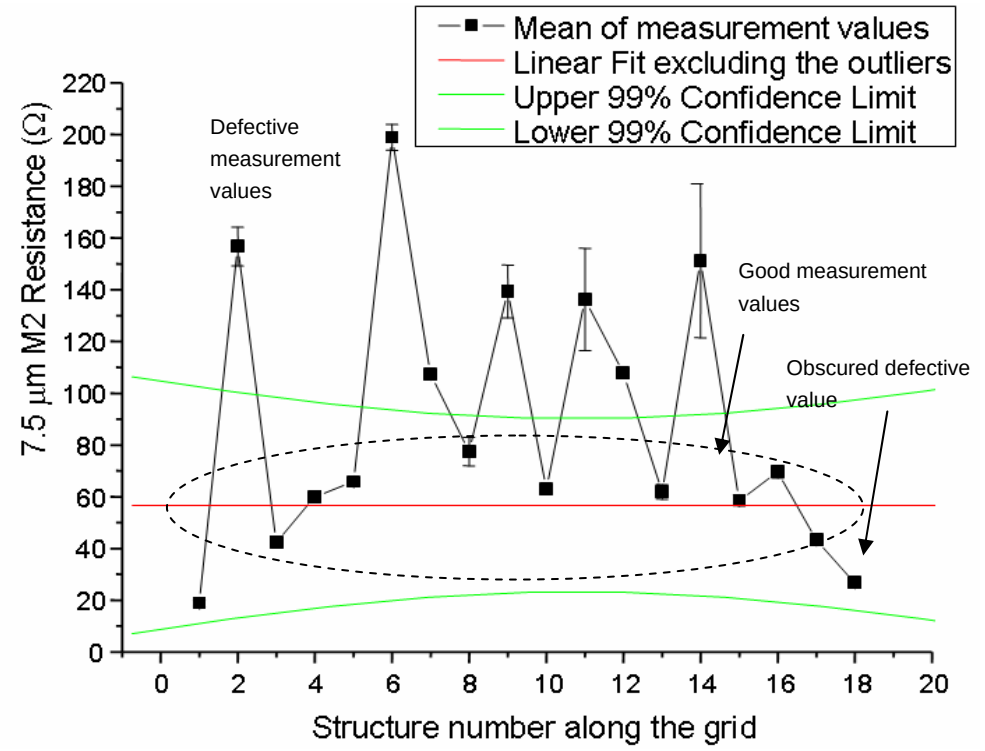

Figure 5.7: Measurement results from the test structure for detecting step-coverage problems in the M2 layer showing the presence of huge parametric variations along the grid positions (JeSEF_1176_10).

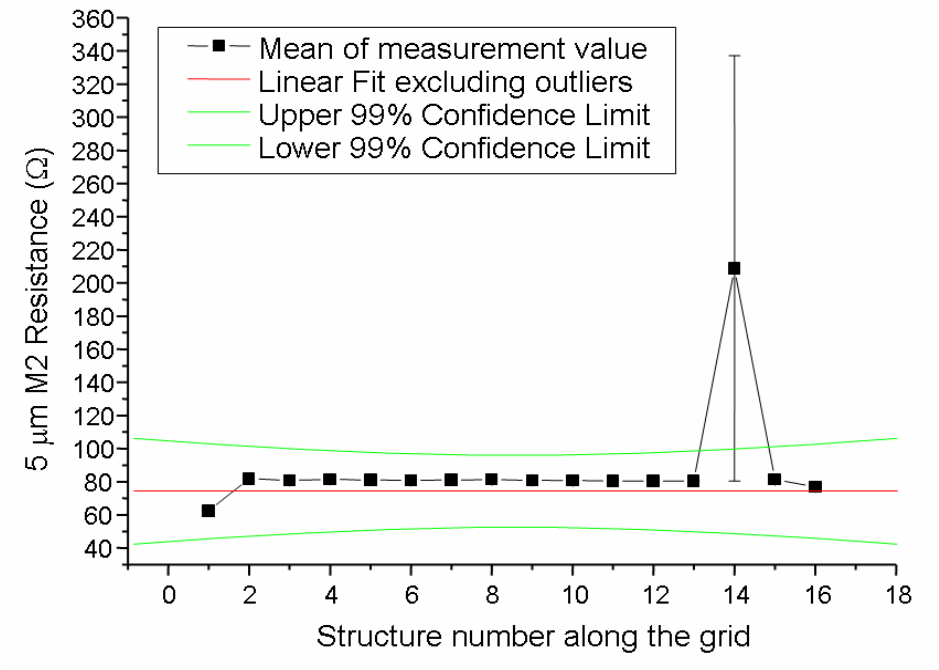

Figure 5.8: Measurement results from the test structure showing the presence of a structural defect – in this case a crack in wiring layer M2 (JeSEF_1202_15).

chip # 10). The width of the M2 wire is 7.5 µm. The analysis is as follows. The average value of the resistance is calculated taking into consideration the possible measurement error as well as the outliers and confidence lines of 99% are drawn from these values. Since the measurement values of a good structure shows a Gaussian distribution caused by normal parametric variation, a confidence interval gives an estimated range of values which is likely to include an unknown population parameter, the estimated range being calculated from a given (limited) set of sample data. If independent samples are taken repeatedly from the same population, and a confidence interval calculated for each sample, then a certain percentage (confidence level) of the intervals will include the unknown population parameter. Confidence intervals are usually calculated so that this percentage is 95% but a confidence interval of 99% can also be calculated as used in this analysis. Confidence limits are the lower and upper boundaries / values of a confidence interval, that is, the values which define the range of a confidence interval.

The slope of the fitted line is fixed to 0 to make sure that the defects have minimum effects on the measured values (exclusion of the outliers). The measurements points lying outside these confidence limits show the presence of a defect in the case of a parametrically good chip. In the case of huge parametric variations, some of the defective values can be obscured as shown in Figure 5.7 due to non-normal distribution of the process variations.

The error will be higher if the structure is being affected by intra-chip parametric variation. As can be seen in Figure 5.7, due to the parametric variation in the chip, the so called error bars become wider for several measurements. Error bars [8] are used to show uncertainty in data values from the statistical point of view. These uncertainties may be caused by measurement errors or instrument noise, and are usually specified in terms of standard deviations away from the data value. To reduce the probability of measurement error, the measurement has been carried out twice. Error bars allow to graphically illustrate actual errors, the statistical probability of errors, or a general approximation or in our case a "spread" in the data. Several of the measurement points lie outside the confidence limit, showing the presence of a parametric influence in defects. Measurement results from a parametrically good chip (JeSEF wafer #1201, chip #15) are given in Figure 5.8. Here the appearance of a structural defect (#14) is prominent. The M2 wire is 5 μm in width in this case. The designed value of the resistance for the structure is 60 Ω in both cases. This value was used for fitting and the resulting mean value is used as the guess value in the algorithm for statistical analysis as presented in Figure 5.6. It also shows the shift in the values of the end structures due to measurement inaccuracy as mentioned in Section 4.4.2 of this thesis. In both case, it is seen that there is a shift in the actual parametric value due to the development nature of the process.

5.3.2 Statistical Analysis of Defect Data

The statistical analysis of the JeSEF measurement data is performed by a MATLAB program as presented in Figure 5.6. The main program has been modified for each test structure according to the allowed process variation (tolerance) of the parameter involved. There are 10 chips in each wafer that have to be tested, since two of the 12 chips in a wafer (shown in Figure 5.2a) are partially populated as explained in the previous chapter of this thesis. An example of the test data sheet with the summary of results from one of the wafers is shown in Table 5.1. The first column shows the position of the chip in the wafer as given in Figure 5.2a. The next six columns provide the statistics of the different structures in each chip. The first sub-column shows the total number of structures tested in each chip. The second sub-column gives the number of defective structures detected and the third sub-column shows the percentage of the defective structures in each chip for the particular type of structure.

The statistics show that the resistor defects, i.e. those of the bias and shunt resistors, are less severe compared to the defects in interconnect. The step-coverage problem of M2 at a via turns out to be the most serious concern among the investigated defects. Table 5.2 shows the summary of the defect statistics of one of the JeSEF wafers, viz. 1175 of version JeSEF_Jan02.

The first column gives the chip number for the data given in columns 2 to 7. The second column shows the statistics for the bias resistor structure and the third column the shunt resistor. The fourth, fifth and the sixth shows the statistics of the meander structures of M2, with wire widths of 5, 7.5 and 10 μm respectively. The seventh column provides the statistics of the via structure. The defect percentage of the bias resistor structure was about 0.7% and that of the shunt resistor about 0.4%, while the M2 meander resistances showed percentages of around 12, 10 and 9 respectively for the 5, 7.5 and 10 μm wires. The via structures exhibited the most critical situation with about 61% of the total structures being defective. This is one of the relatively good wafers received from JeSEF in terms of process spread leading to less parametric defects in the test chips.

Forty chips from four different wafers were used for the analysis of the JeSEF process. The (limited) statistic data of the JeSEF process is given in Table 5.3 which also includes the results from bad chips which exhibit large parametric variations. The organization of the table is the same as that of Table 5.2 given above.

Table 5.1: Results showing the details of defect data from a JeSEF Wafer (JeSEF_Jan02 #1175).

Chip no	Bias R			Shunt R			M2 meander with line width									Via		
							5 µm			7.5 µm			10 µm					
	Total	Defective	%	Total	Defective	%	Total	Defective	%	Total	Defective	%	Total	Defective	%	Total	Defective	%
8	1088	2	0.18	1088	4	0.37	256	39	15.23	192	20	10.42	192	20	10.42	320	182	56.88
9	1088	4	0.37	1088	10	0.92	256	37	14.45	192	15	7.81	192	19	9.90	320	191	59.69
10	1088	5	0.46	1088	2	0.18	256	30	11.72	192	20	10.42	192	14	7.29	256	133	51.95
14	1088	8	0.74	1088	2	0.18	256	22	8.59	192	16	8.33	192	19	9.90	256	123	48.05
15	1088	1	0.09	1088	4	0.37	224	16	7.14	192	40	20.83	192	16	8.33	256	196	76.56
17	1088	0	0	1088	1	0.09	256	42	16.41	192	14	7.29	192	15	7.81	256	231	90.23
18	1088	0	0	1088	0	0	256	29	11.33	192	13	6.77	192	14	7.29	256	221	86.33
19	1088	44	4.04	1088	13	1.20	256	32	12.50	192	17	8.86	192	19	9.90	320	106	33.13
23	1088	0	0	1088	0	0	256	29	11.33	192	14	7.29	192	19	9.90	256	146	57.03
24	1088	7	0.64	1088	8	0.74	256	20	7.81	192	14	7.29	192	20	10.42	320	157	49.06

Table 5.2: Summarised statistics of the JeSEF_Jan02 Wafer 1175.

TOTAL	Bias R	Shunt R	M2 meander of width			Via
			5 μm	7.5 μm	10 μm	
Number	10880	10880	2528	1920	1920	2816
Defective	71	44	296	183	175	1686
% Defect	0.65	0.40	11.65	9.53	9.12	60.89

The statistics show that the percentage of defects for the resistor structures has increased to 3% for the bias resistors and 6% for the shunt resistors while the percentage of the M2 meander increased to about 15% and 14% respectively for the 5 and 7.5 μm wiring and about 18% for 10 μm wires. The percentage of the defective via structures was reduced to about 58% in the total statistics. The change of the defect percentage is 77, 93, 25, 40, 100 and 5% for bias, shunt, 5 μm, 7.5 μm, 10 μm meander and via structures. This shows that a via defect is mostly independent of the parametric variation involved in other defects. The high percentage of the detected defects in the measured via structures shows that this is a prominent defect in the JeSEF process.

Table 5.3: Overall statistical results of the JeSEF Process from 4 wafers.

TOTAL	Bias R	Shunt R	M2 meander of width			Via
			5 μm	7.5 μm	10 μm	
Number	45144	45120	9984	7904	7968	10454
Defective	1227	2583	1482	1109	1449	6053
% Defect	2.72	5.73	14.84	14.03	18.19	57.90

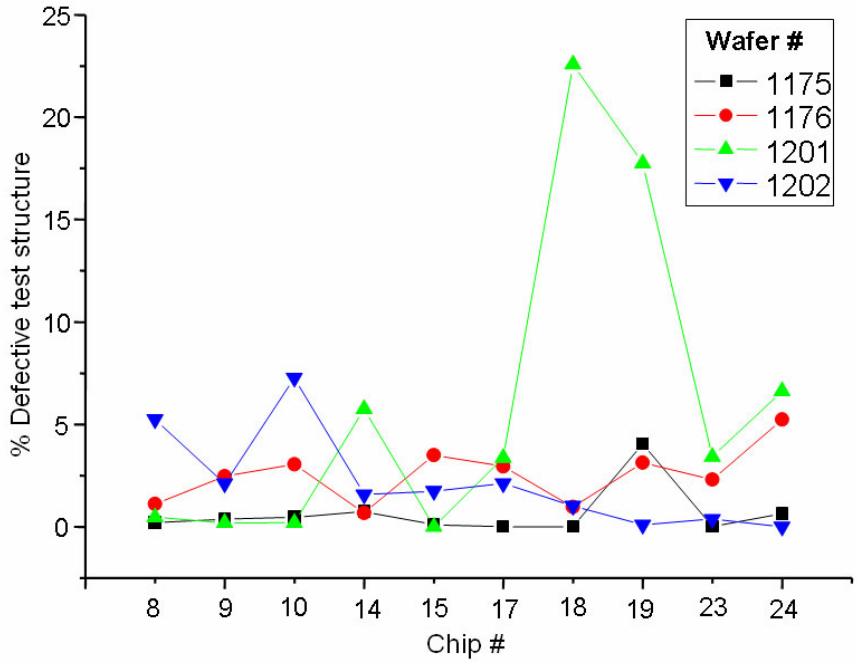

Figure 5.9: Results of the test structure for the bias resistor from the four JeSEF wafers showing the variation of defects in them.

Another phenomenon to be explained is the reversal of the percentage of defects for the meander structures as follows. In general, the statistics from the good wafer JeSEF_Jan02 #1175 (Table 5.1) showed progressively decreasing defect statistics for the M2 wires of 5, 7.5 and 10 μm respectively. For the total statistics (all wafers), this was reversed. This is due to the fact that the probability of the occurrence is directly proportional to the critical area as well as inversely proportional to the minimum size of the structure. As the size of a test structure increases, the critical area increases. The critical area is defined as the area of a die on which if the center of a defect of a given size (assuming a circular defect) lands it will cause a short [9]. Therefore, there will be a unique critical area for each defect size and for each layer in the die. The critical area increases monotonically with the defect size and saturates once it reaches the layout area.) In the presence of huge process variations in the realization, the critical area plays a more dominant role than in the case of the parametrically good case. A summary of the statistics is presented in the following graphs.

Figure 5.9 shows the statistics of the bias resistor structure. The number on the x-axis corresponds to the position number of the chip in Figure 5.2a. % defective structure refers to the percentage of the structures in which a defect was found. The graph shows that chips 18 and 19 of the JeSEF wafer JeSEF_Jan02 #1201 had relatively more defects than the rest of the chips. The adjacent chips 14 and 24 also have relatively higher defects; hence this could be due to a parametric defect in this part of the wafer.

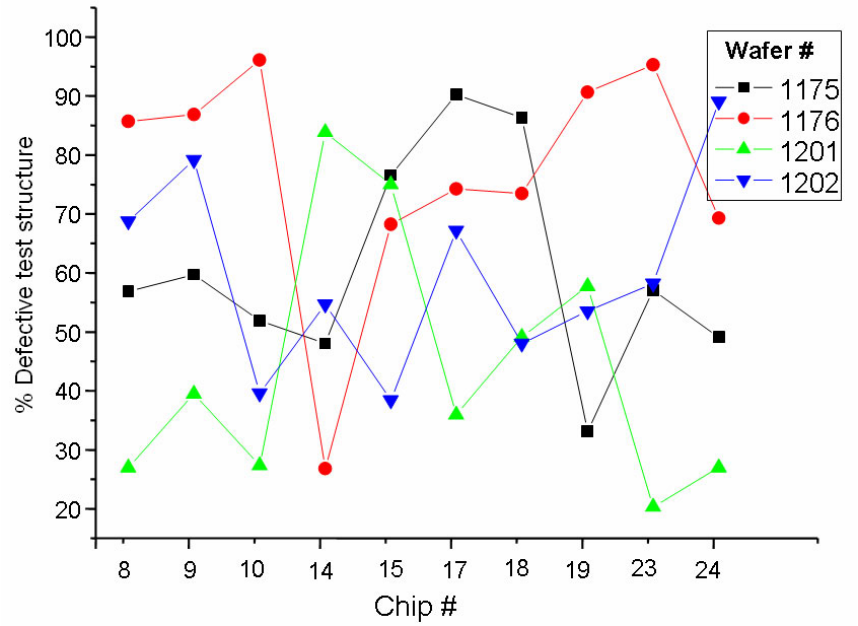

Figure 5.10: Measurement results of the test structure for detecting step-coverage problems over a via in the JeSEF process showing a huge variation in the occurrence of defect.

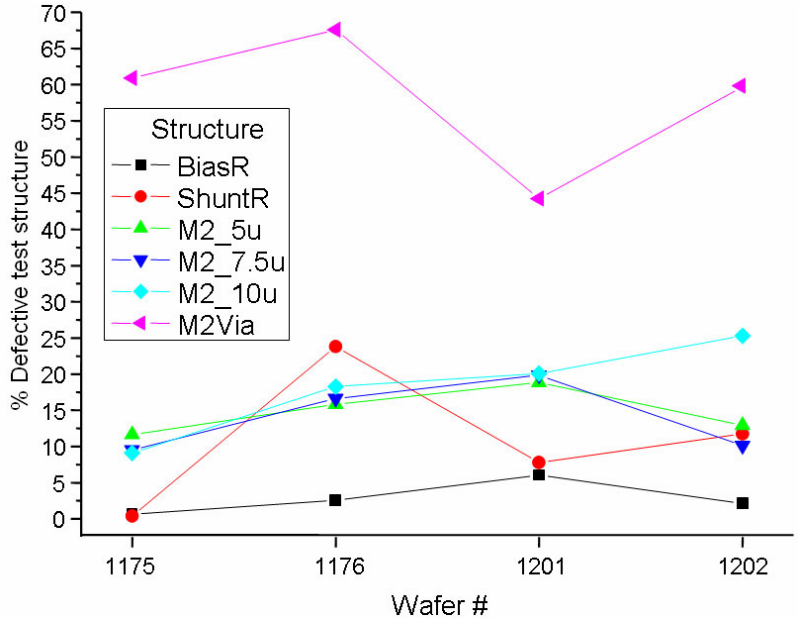

Figure 5.11: Summary of results on the test structures for the JeSEF process showing the immature nature of the process.

Figure 5.10 shows the statistics of the via structure, which exhibits the most serious defects detected in the JeSEF process. The x-axis shows the position of the chip as before. The variation of the defect percentage is between 20% in the JeSEF wafer #1201 up to 95% in #1176. This shows that step-coverage of the M2 layer over a via is a serious concern in the process.

Figure 5.11 shows the summary of the measurement results with regard to the four JeSEF wafers. The x-axis shows the wafer number and on the y-axis the percentage defects of each structure is provided. This graph clearly shows the critical nature of the via defects in the JeSEF process as well as the immature nature of the JeSEF process.

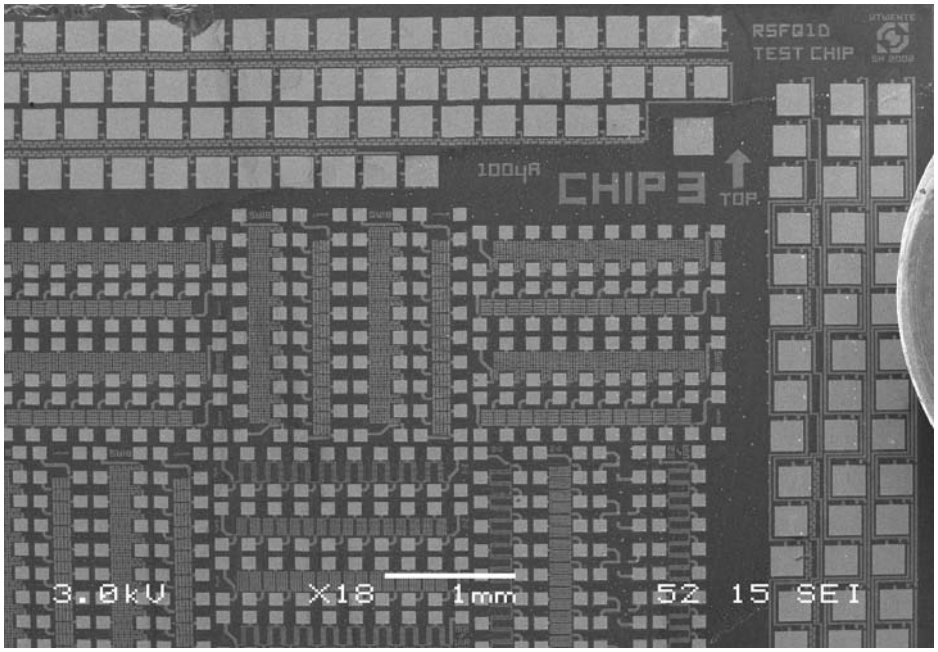

Figure 5.12: A SEM photograph of a part of one of the realised JeSEF chips showing the RT structures in the centre and the LT structures in the top and right periphery.

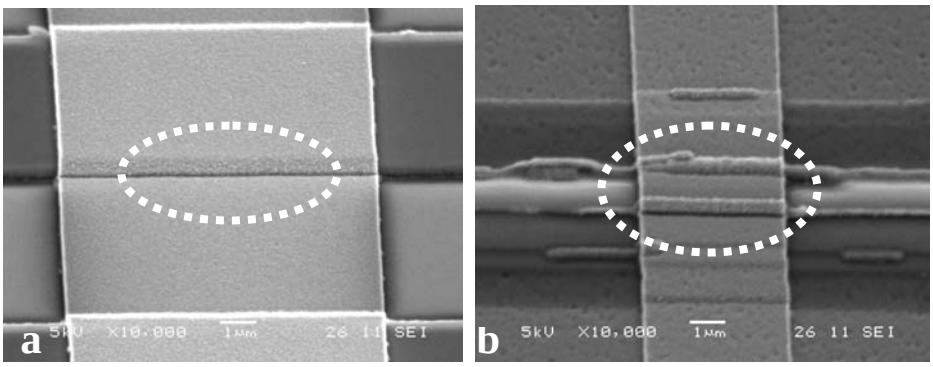

Figure 5.13: SEM photographs of the detected defects in the chips developed for the JeSEF process: a) an M2 meander showing the step-coverage over an M1 edge b) a via structure showing some residue material causing the defect.

A SEM photograph of part of the realized chip for the JeSEF process is shown in Figure 5.12. The RT structures can be seen towards the centre and the LT structures in the top and right periphery of the chip. Two examples of the detected defects are shown in Figure 5.13. Figure 5.13a shows a step-coverage problem in the M2 meander over an M1 edge and Figure 5.13b shows one of the defective via structures showing the residue of underlying step and causing the defect.

5.4 Analysis of the HYPRES Process

As mentioned in the previous chapter of this thesis, the number of the same type of test structures was reduced in the HYPRES design and more structures of different types were incorporated into the test chip [10], [11]. Again the number of chips per wafer had to be reduced due to the high cost of realisation at this commercial foundry. These facts have affected the analysis of the HYPRES process. Primarily, the wafer maps as in the case of the JeSEF process could not be carried out because of limited information per chip. But the advantage was that information about more different defects is available from the test chips. Since the foundry is taking care of the process variations using their own parametric test structures, the information lost in reducing the number of chips is not relevant as the same information is available at the foundry. This information is not included in this thesis due to a non-disclosure agreement.

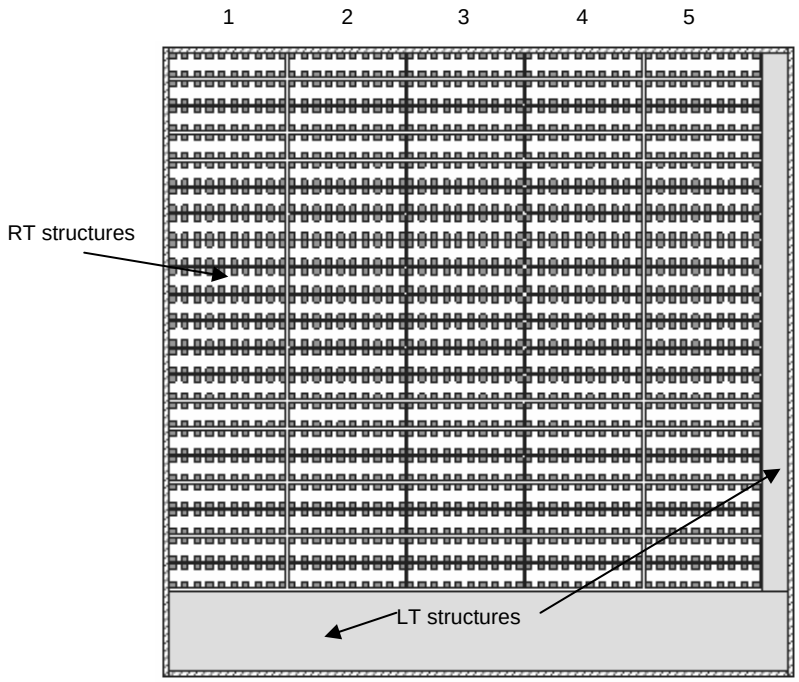

Figure 5.14: Outline of the HYPRES test chip (HYPRES_Nov03) showing the RT structures on the major part and the LT structures on the lower part and the defect-induced JJ structures on the right edge.

Three test chips were incorporated in each wafer and the outline of the test chip is as shown in Figure 5.14. There are 100 sets of structures in each chip exclusive for room-temperature (RT) measurement. They are divided into 5 columns of 20 sets of structures as shown in the Figure 5.14. The test time required by the prober to complete the data acquisition from a single test chip is about 80 minutes. The room temperature tests were carried out at 298 K using the temperature controller module in the experimental set-up.

The analysis of the measurement data was similar to the JeSEF process, as described in Section 5.3 of this chapter, except that the process variation is much less compared to the JeSEF process. A modified version of the script for the algorithm presented in Figure 5.6 was used for the analysis. As in the case of the JeSEF process, the script was customised for each type of test structure, e.g. to change the tolerance limits.

Table 5.4: Statistics of measurement data of the HYPRES Wafer 665.

#	Structure	Chip 1			Chip 2			Chip 3		
		#	D	%	#	D	%	#	D	%
1	R2M2Bdg	306	0	0	306	0	0	204	0	0
2	M3M2BdgM2M1	340	0	0	340	0	0	204	0	0
3	M3M2BdgM2	306	0	0	306	0	0	204	0	0
4	M2M1BdgM1	306	6	1.96	306	0	0	204	0	0
5	M3M2Via_3u	96	64	66.67	96	70	72.92	64	63	98.44
6	M3M2via_2u	144	14	9.72	144	18	12.50	96	20	20.83
7	M3M1Via_3u	96	82	85.42	96	68	70.83	64	28	43.75
8	M3M1via_2u	112	58	51.79	112	70	62.50	96	47	48.96
9	M3M0Via_3u	96	6	6.25	96	6	6.25	64	9	14.06
10	M3M0via_2u	144	1	0.69	144	3	2.08	96	2	2.08
11	M2M1Via_3u	96	0	0	96	0	0	64	6	9.38
12	M2M1Via_2u	144	0	0	144	0	0	96	8	8.33
13	M2M0Via_3u	96	6	6.25	96	6	6.25	64	8	12.50
14	M2M0Via_2u	144	9	6.25	144	6	4.17	96	7	7.29
15	M1M0Via_3uM2	96	0	0	96	0	0	64	2	3.13
16	M1M0Via_2uM2	144	0	0	144	0	0	96	4	4.17
17	M1M0Via_3u5	96	6	6.25	96	6	6.25	64	6	9.38
18	M1M0Via_2u5	144	0	0	144	3	2.08	96	4	4.17
19	M3_4uM2	96	0	0	96	0	0	64	8	12.50
20	M3_3uM2	96	0	0	96	0	0	64	6	9.38
21	M3_2uM2	144	0	0	144	3	2.08	96	5	5.21
22	M3_2uM2M1	96	0	0	96	0	0	64	7	10.94
23	M2_4uM1	96	0	0	96	0	0	64	7	10.94
24	M2_3uM1	96	0	0	96	0	0	64	2	3.13
25	M2_2uM1	144	0	0	144	0	0	96	2	2.08

Example data from one of the relatively good HYPRES wafers is shown in Table 5.4. The data is from HYPRES wafer #665. The column labelled “structure” gives the name of the structures which were described in Chapter 3 and 4 of this thesis. They are grouped in rows based on the nature of the defect involved. The first group is for the interlayer shorts (1 - 4 in Table 5.4) followed by the group for the step-coverage problems over a via (5 - 18 in Table 5.4) and step-coverage over an edge (19 - 25 in Table 5.4). The three main columns represent data from the three different test chips in the wafer. The three sub-columns represent the following: the total number of structures tested, is labelled by ‘#’, the number of detected defective structures ‘D’ and the percentage of defective structures

‘%’. As seen in the table (shadowed areas), some of the structures are heavily affected. These defects are caused by an error in one of the layers (R3), the Pd-Au top layer which is being used for bonding as well as the implementation of low-value resistances. In this case, the layer R3 was under-etched, by which the remnants caused shorting of the test structures. A less number of defects in the M3M2via_2u via (row #6) also explain this error as the probability is less for the R3 layer residue to be present in this structure (relative smaller dimension in terms of area and step height). It also shows that chip 3 was the worst affected probably because it is an edge die.

The total statistics of the same wafer is presented in Table 5.5. The first column denoted by ‘#’ denotes the reference number of the structure to be later used in the analysis. The second column gives the name of the corresponding structure whose statistics are shown in the subsequent columns. The total number of structures tested is followed by the number of defective structures and the percentage of the detected defects is shown in the third, fourth and the fifth columns respectively. The defects in the M3-M2 and the M3-M1 vias are prominent (shaded) due to the under-etch error in the layer R3 as mentioned before.

Test chips from eight wafers were received from HYPRES. This represents a production span of five months for the foundry. It has to be noted that these wafers have been released in the months immediately after the renovations in the HYPRES foundry. Some of the high percentage of the defects could be due to this or might have influenced the process. Twenty-three test chips were tested at room temperature, from the eight wafers. All of the predicted defects have been detected in at least one of the test chips. A summary of the complete test result on the HYPRES process is presented in Table 5.6

Table 5.5: Summary of the measurement results of HYPRES wafer #665.

#	Structure	Number Tested	Number Defective	% Defect
1	R2M2Bdg	816	0	0
2	M3M2BdgM2M1	884	0	0
3	M3M2BdgM2	816	0	0
4	M2M1BdgM1	816	6	0.74
5	M3M2Via_3u	256	197	76.95
6	M3M2via_2u	384	52	13.54
7	M3M1Via_3u	256	178	69.53
8	M3M1via_2u	320	175	54.69
9	M3M0Via_3u	256	21	8.20
10	M3M0via_2u	384	6	1.56
11	M2M1Via_3u	256	6	2.34
12	M2M1Via_2u	384	8	2.08
13	M2M0Via_3u	256	20	7.81
14	M2M0Via_2u	384	22	5.73
15	M1M0Via_3uM2	256	2	0.78
16	M1M0Via_2uM2	384	4	1.04
17	M1M0Via_3u5	256	18	7.03
18	M1M0Via_2u5	384	7	1.82
19	M3_4uM2	256	8	3.13
20	M3_3uM2	256	6	2.34
21	M3_2uM2	384	8	2.08
22	M3_2uM2M1	256	7	2.73
23	M2_4uM1	256	7	2.73
24	M2_3uM1	256	2	0.78
25	M2_2uM1	384	2	0.52

which again shows the influence of the previously mentioned error in the results. The format of this table is the same as that of the previous table.

A histogram of the percentage defective structures is shown in Figure 5.15. This histogram summarises the measurement results. The number on the x-axis corresponds to the reference number of the structures as given in Table 5.5 and Table 5.6. The y-axis can be considered as a measure for the defect density in the process. It shows that the HYPRES wafers #671 and #672 (dark bars) suffered from many defects. This was due to the fact that

Table 5.6: Statistical results of the HYPRES process from 8 wafers.

#	Structure	Number Tested	Number Defective	% Defect
1	R2M2Bdg	5100	4	0.08
2	M3M2BdgM2M1	5168	1122	21.71
3	M3M2BdgM2	5100	1122	22.00
4	M2M1BdgM1	5100	22	0.43
5	M3M2Via_3u	1600	876	54.75
6	M3M2via_2u	2368	1118	47.21
7	M3M1Via_3u	1632	1079	66.12
8	M3M1via_2u	2336	1323	56.64
9	M3M0Via_3u	1552	590	38.02
10	M3M0via_2u	2400	655	27.29
11	M2M1Via_3u	1600	59	3.69
12	M2M1Via_2u	2368	42	1.77
13	M2M0Via_3u	1600	199	12.44
14	M2M0Via_2u	2400	135	5.63
15	M1M0Via_3uM2	1600	208	13.00
16	M1M0Via_2uM2	2400	318	13.25
17	M1M0Via_3u5	1600	78	4.88
18	M1M0Via_2u5	2400	53	2.21
19	M3_4uM2	1600	423	26.44
20	M3_3uM2	1600	393	24.56
21	M3_2uM2	2400	564	23.50
22	M3_2uM2M1	1600	383	23.94
23	M2_4uM1	1600	76	4.75
24	M2_3uM1	1600	52	3.25
25	M2_2uM1	2400	43	1.79

there was a (process) error in the deposition of the insulation layer I2 for those wafers. It also shows that the structures involving the layer M3 for step-coverage over vias has a high probability of defects as seen in structures numbered from 5 to 10 (shown by arrow).

Summarising the above discussion, a ranking of the defect-prone locations in the HYPRES process is given in Table 5.7, resulting from the investigations on the process. The first column shows the ranking of the defect given in the third column. The second column shows the name of the structure and the fourth column the percentage of the detected defects. As mentioned before, the top ranking defect-prone locations involve the wiring layer M3 (shaded). This could be due to the fact that the error in both the layers R3 and I2 influenced the layer M3 as it is the adjacent layer to both. The step-coverage problem over a via remains as the predominant defects as predicted before in Chapter 4 of this thesis. The highest ranking defect location, a crack in the M3 layer over a 3μ M3M1 via, showed that 66% of the total structures tested were defective. The least detected defect, a short between the M2 and R2 layers over an R2 edge, showed that about 0.08% of the total structures were defective. This last ranked defect is a condition that violates the HYPRES design rules, but was observed in certain library cells as presented in Chapter 4 of this thesis.

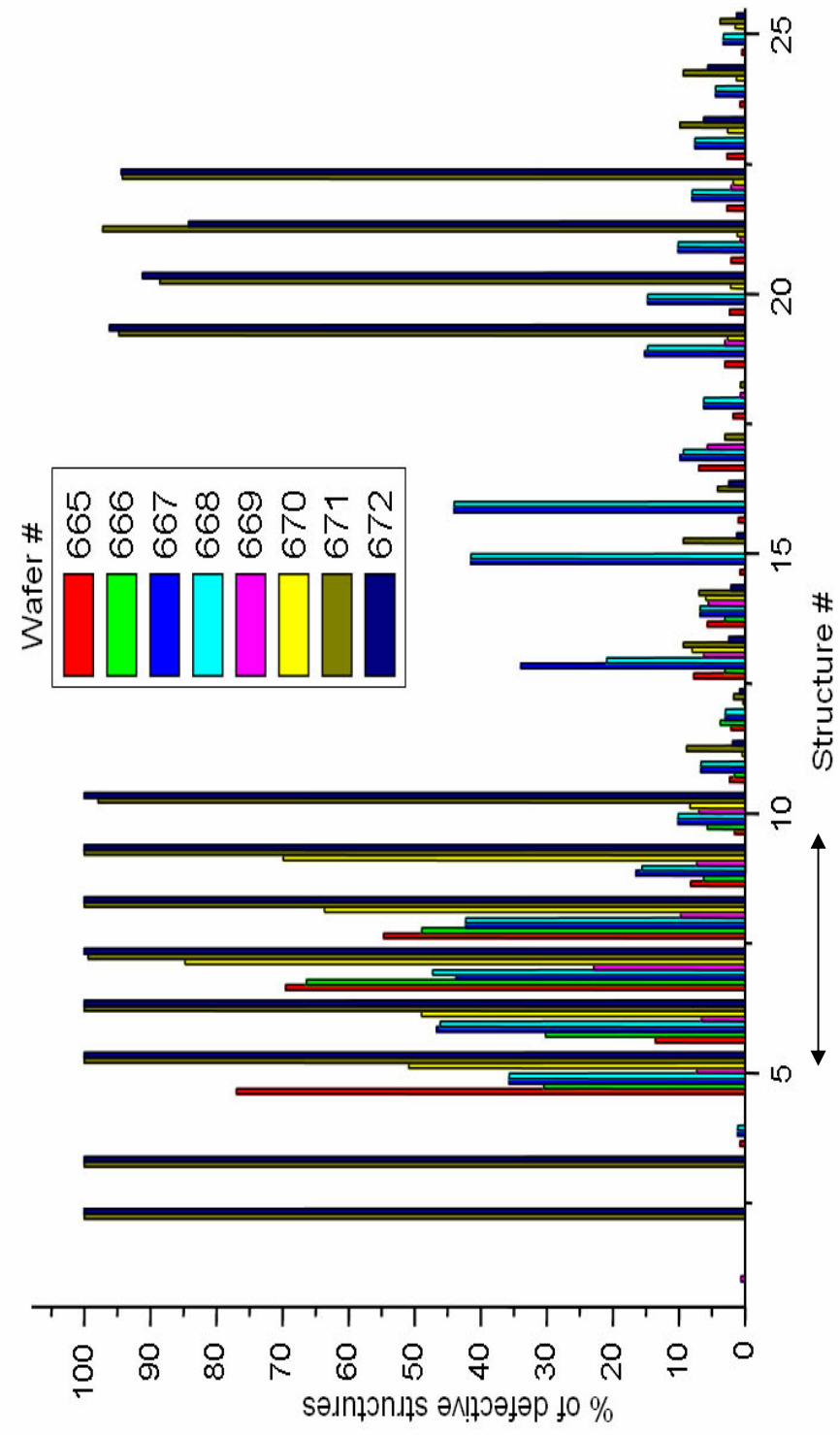

Figure 5.15: Measurement results on defective test structures for the HYPRES process for different wafers.

Table 5.7: Ranking of the defect-prone locations in the HYPRES Process

Rank #	Structure	Resulting Defect	Defect %
1	M3M1Via_3u	M3 crack over a 3μ M3M1 via	66.12
2	M3M1via_2u	M3 crack over a 2μ M3M1 via	56.64
3	M3M2Via_3u	M3 crack over a 3μ M3M2 via	54.75
4	M3M2via_2u	M3 crack over a 2 M3M2 via	47.21
5	M3M0Via_3u	M3 crack over a 3μ M3M0 via	38.02
6	M3M0via_2u	M3 crack over a 2 M3M0 via	27.29
7	M3_4uM2	Crack in 4μ M3 over an M2 edge	26.44
8	M3_3uM2	Crack in 3μ M3 over an M2 edge	24.56
9	M3_2uM2M1	Crack in 2μ M3 over an M2M1 edge	23.94
10	M3_2uM2	Crack in 2μ M3 over an M2 edge	23.50
11	M3M2BdgM2	Short between M3 & M2 over M2 edge	22.00
12	M3M2BdgM2M1	Short between M3 & M2 over M2M1 edge	21.71
13	M1M0Via_2uM2	M2 crack over a 2μ M1M0 via	13.25
14	M1M0Via_3uM2	M2 crack over a 3μ M1M0 via	13.00
15	M2M0Via_3u	M2 crack over a 3μ M2M0 via	12.44
16	M2M0Via_2u	M2 crack over a 2μ M2M0 via	5.63
17	M1M0Via_3u5	M1 crack over a 3.5μ M1M0 via	4.88
18	M2_4uM1	Crack in 4μ M2 over an M1 edge	4.75
19	M2M1Via_3u	M2 crack over a 3μ M2M1via	3.69
20	M2_3uM1	Crack in 3μ M2 over an M1 edge	3.25
21	M1M0Via_2u5	M1 crack over a 2.5μ M1M0 via	2.21
22	M2_2uM1	Crack in 2μ M2 over an M1 edge	1.79
23	M2M1Via_2u	M2 crack over a 2μ M2M1 via	1.77
24	M2M1BdgM1	Short between M2 & M1 over M1 edge	0.43
25	R2M2Bdg	Short between M2 & R2 over R2 edge	0.08

The summary of the statistical results is graphically presented in Figure 5.16. The x-axis represents the wafer number and the y-axis the percentage of the detected defects in various structures. The average value of the defect percentage per wafer for each structure was used for the data points. The detected process problems can be clearly identified as peaks in the graph. Four regions are marked in the graph which showed high defect detection. The region marked '1' resulted from the under-etch problem described earlier. M3M2 and M3M1 via structures were affected by this problem. In region '2', the under-etch problem is still present but to lesser extent after the problem was identified. Wafer # 669 was a better wafer but one of the chips were affected with the under-etch probably due to its location close to the edge of the wafer. Region '3' shows the problem re-appearing in wafer 670. Finally region '4' shows the isolation layer (I2) problem mentioned before.

A graph showing the total statistics for the HYPRES process is given in Figure 5.17. The measurement results from all eight wafers were used to generate this graph. The x-axis corresponds to the reference number of the structures as given in Table 5.5 and Table 5.6. The y-axis shows again the percentage of detected defective test structures. The big peak marked in the graph (structures 5 - 10) represents those structures developed for the M3 metal step-coverage over different vias as mentioned earlier. The smaller peaks marked are due to the influence of the I2 isolation problem in the defects.

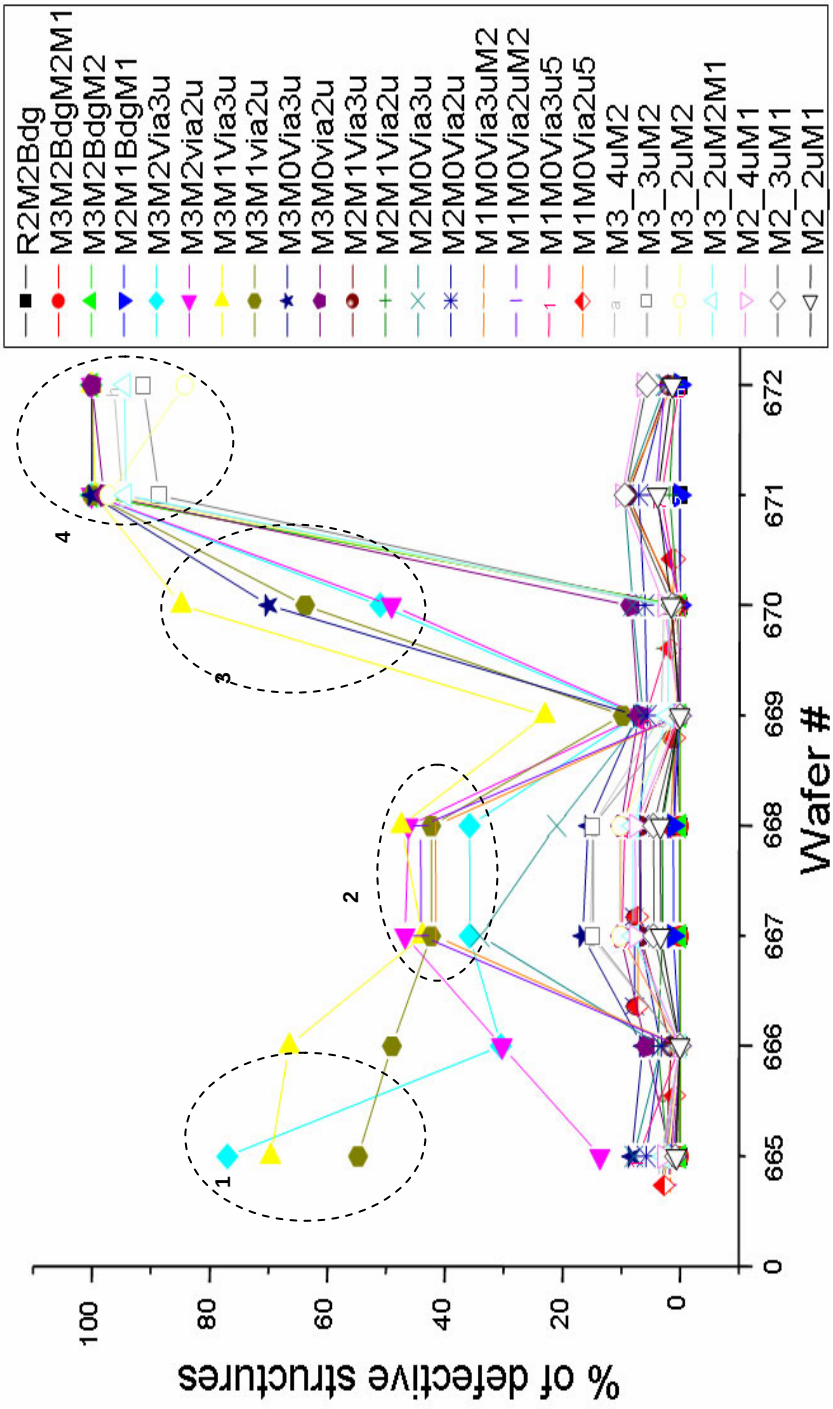

Figure 5.16: Summary of results on the test structures for the HYPRES process for different wafers (see text).

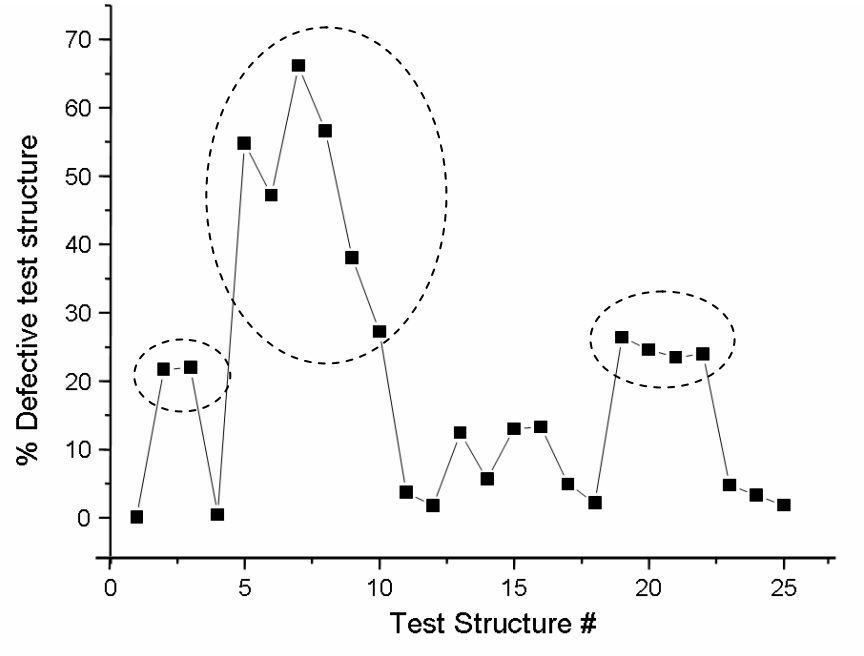

Figure 5.17: Complete results on test structures for the HYPRES process for all the measured eight wafers (Table 5.6 and Table 5.7 give the details of the test structures).

A SEM photograph of one of the realised chips for the HYPRES process (HYPRES_Nov03) is given in Figure 5.18a and a photo-micrograph of a part of the same chip for the process is given in Figure 5.18b. The RT test structures can be seen in the top portion and the LT structures on the lower side and the right edge of the chip.

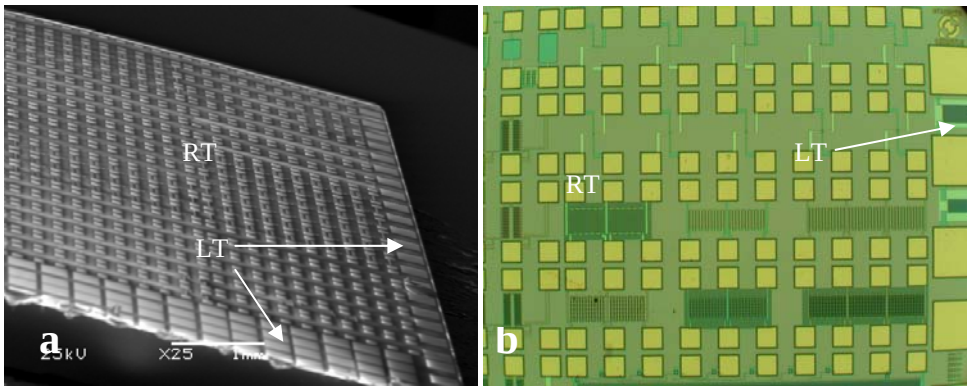

Figure 5.18: A SEM photograph (a) and a micro-photograph (b) of one of the realised HYPRES test chips (HYPRES_Nov03) showing the RT and LT structures.

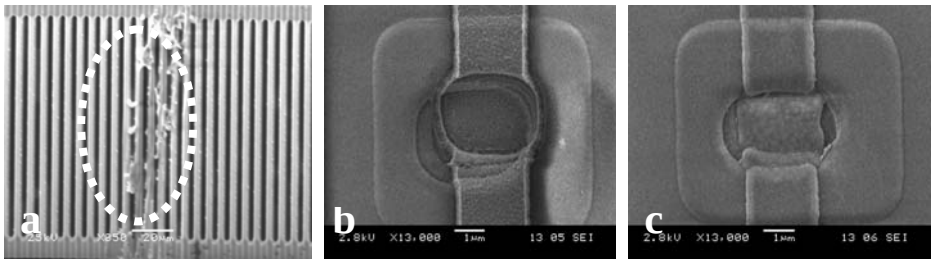

Figure 5.19: SEM photographs of the detected defects in the chips developed for the HYPRES process: a) a shorted M3-M2 meander, b) an M3-M0 via showing step-coverage problem and c) a cracked M2 wire over an M2-M0 via.

Three examples of detected defects are shown in Figure 5.19. They were found after a visual inspection of the corresponding defective structure after the measurements. Figure 5.19a shows an interlayer short between the M3 and M2 layers. Figure 5.19b shows an M3 step-coverage problem in the M3-M0 via (a misalignment is also visible) and Figure 5.19c shows one of the defective M2-M0 via structures showing M2 wire cracking.

It was also clear from the results that the process is not that mature as it was claimed to be. Constant development activities were going on during the investigation. After realising the weak points of the process from us, HYPRES changed some process steps (introduction of an additional anodisation layer and change in the order of mask) and tightened the DRC checks at the foundry as well as revision of design rules. As a result, the investigation has to be repeated for the new ranking list of defects. This could not be carried out due to time limitations.

5.5 Measurement Techniques at Low Temperatures

The previous sections described the RT measurement methodology and the analysis of both the RSFQ processes under investigation. This defect information will be useful for inductive fault analysis while developing an ATPG approach for RSFQ circuits [12]. Some of the preliminary results will be presented in the next chapter.

In this section, the test methodologies used for low-temperature measurements are presented [13]. The details of the JJ structure design have been presented in chapters 3 and 4 of this thesis. For a better understanding of this section, the following references are recommended [14] - [18].

The original idea was to implement the scheme as described in reference [1]. The proposed setup to be used for the experiments is as shown in Figure 5.20. It consists of a differential power supply for the superconducting coil (to be used for inducing a magnetic field (B) for the I_c-B experiment described in [1]), the chip mounted on an RF-shielded cryo-probe in a liquid-Helium dewar and a parameter analyser HP4156B for the analysis. The reason for using this parameter analyzer is to speed up the detection of the defects by reducing the test time, as it is able to program the force current and measure the voltage

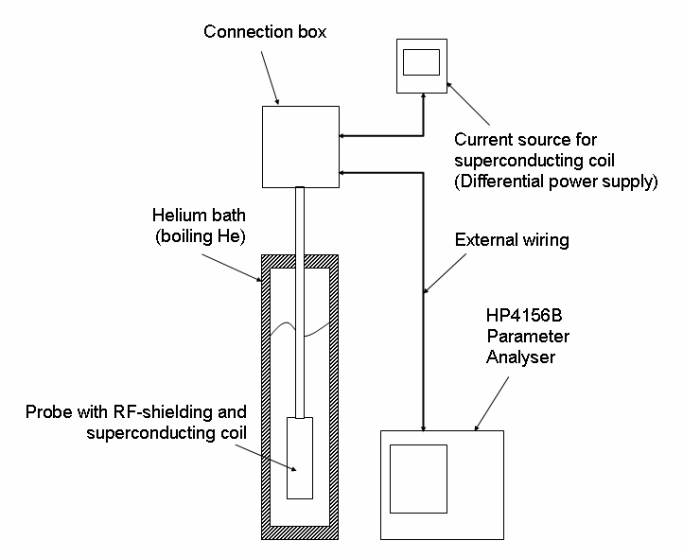

Figure 5.20: Proposed setup for the detection of defects in a Josephson junction using I-V measurements on a JJ string.

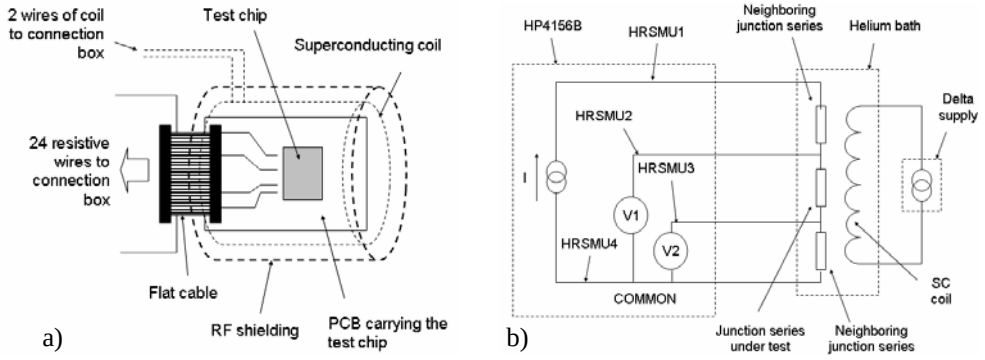

Figure 5.21: Parts of the setup in detail: a) connection of the chip to the probe and the shielding employed. b) The schematic for the measurement set-up using an HP4156B parameter analyser.

and record the data. The chip has to be bonded to a PCB and mounted on the cryo-probe as shown in Figure 5.21a. The schematic of the measurement set-up is shown in Figure 5.21b. There are only 24 copper wires in the probe for connections from the PCB to the connection box which limits the number of chains that can be connected at a time to a maximum of 11. This is being limited by the special selector switch on the connection box. Since 4-point measurements are carried out, the resistance of the copper connection wires does not pose any problem. Further details of the setup and precautions for mounting can be found in [1].

One precaution while cooling the chip is to avoid stray magnetic flux-trapping [19]. There is a huge temperature difference while cooling to 4 K from RT and the cooling is not always uniform as there is a huge bulk to be cooled in the process. While on recooling, the probe is lifted so that the chip is slightly above the liquid Helium and slowly inserted back. In this way, the chip is just outside its superconducting temperature (~10 K) while recooling and trapping of flux is easily avoided as the cooling is more uniform by this technique. This recooling technique is always used to make sure that there is no trapped flux in the chip.

The scheme proposed in Figure 5.20 and Figure 5.21 was implemented for the defect analysis of the JJ structures in the realised test chips. The chips were manually wire bonded to the test-access pads as described in Chapter 4 of this thesis. The presence of background noise was initially evident in the measurements. Figure 5.22 shows an example I-V plot obtained while experimenting with an HP4156B. The dotted circle shows a gradual increase of the current showing multiple switching in the JJ chain. In the case of a good series, there will be only one switching equivalent to the I_c of the JJ chain [14]. The slope on the first leg of the graph also shows gradual switching of JJs, which should be a vertical straight line in the case of good JJs. In the case of parametric spread, the JJs can switch sequentially from the one with the lowest I_c to the highest I_c. Any deviation could also shows trapping of fluxes in the JJ chains. During this experiment, all JJs were not switching at the same instance and the number of JJs switching changed after recooling from time to time for the same JJ chain. Hence it can be concluded that this behaviour is neither due to a defective JJ nor parametric spread but to background noise-induced flux trapping.

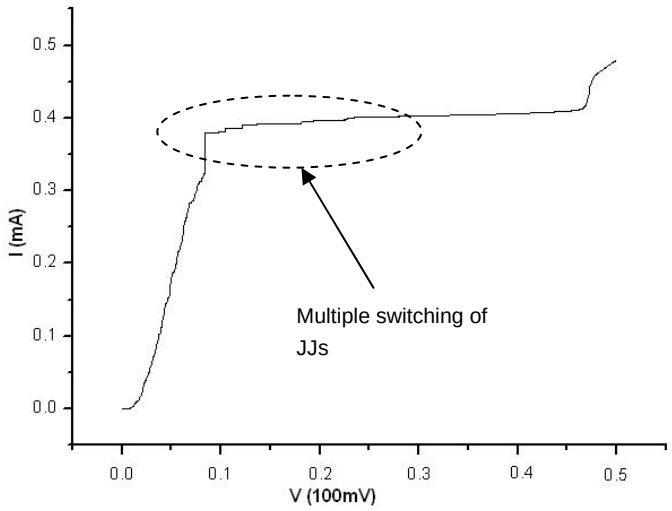

Figure 5.22: An I-V plot from an HP4156B semiconductor parameter analyser showing multiple switching in the JJ series (1 division in x-axis = 10 mV).

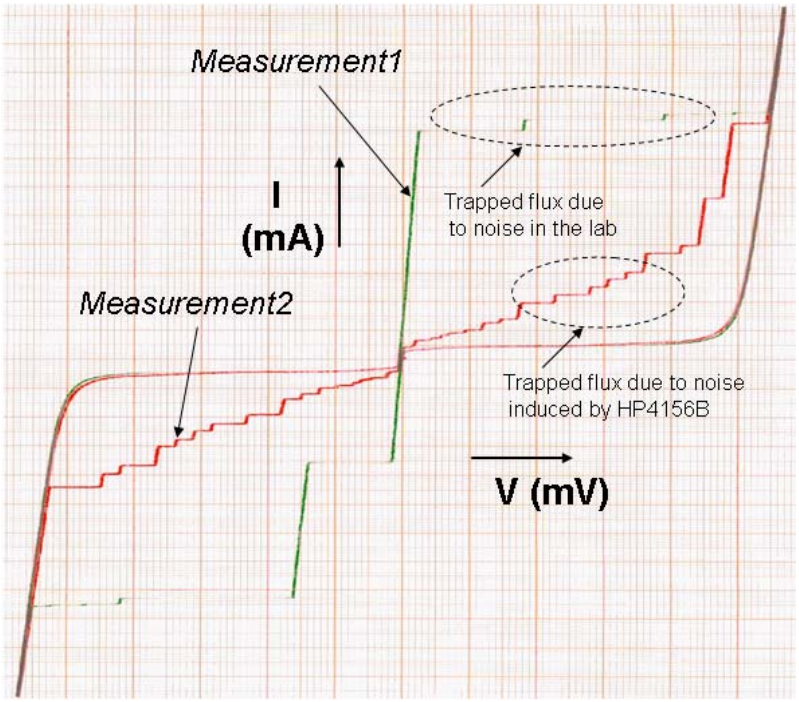

Figure 5.23: Repeated I-V plot measurement (before and after using an HP4156B) with an analogue plotter for the same JJ series showing the induced noise (gradual switching of individual JJs due to trapped flux on both positive and negative branches) from an HP4156B semiconductor parameter analyser (not to scale – in arbitrary units).

As the amount of trapped fluxes varied from time to time, it is not possible to determine whether the shift in the switching moment is due to parametric spread or trapped fluxes or the presence of a defect in a JJ chain by a single LT measurement. As a result of this, it was concluded that presence of a defect can not be verified with this experiment and more study is required to circumvent this problem. This is presented in the following paragraphs.

After a detailed study it was found that the parameter analyser 4156B was also inducing noise into the JJ chains. This is shown in Figure 5.23 on arbitrary scale to prove the situation. It is plotted in arbitrary scale as additional information is not required at this point as it is only for the purpose of comparison. The curve marked “measurement1” shows the measured I-V plot of a series of JJs. This was carried out as follows. The power supply is a sine-wave modulated DC to create a ramp-voltage for the JJs to obtain its I-V curve. A standard ramp generator used for SCE measurements, a Superconducting QUantum Interference Device (SQUID) amplifier setup was used for this and the measurement was carried out using an analogue plotter connected to the connection box replacing the HP4156B (see Figure 5.20). A more detailed treatment of the SQUID measurement

electronics is available in [20]. This plot also shows the noise-induced switching of JJs in the laboratory as they could not be removed even after repeated recooling. After the first measurement, the parameter analyser is used for defect detection. The curve marked “measurement2” is the re-plot of the same I-V curve after the use of an HP4156B. On replotting, it can be seen that almost each JJ in the chain had switched independently. Hence, the curve shows a large amount of flux trapped in the JJs between the two measurements. Hence, it was concluded that the parameter analyser is not suitable for our sensitive measurements.

Further measurements were carried out using a fast Tektronix scope TDS 7404 [21] to evaluate the effects of background noise in the laboratory detected by the previous experiments. A sample plot is shown in Figure 5.24. The small vertical lines on the top side of the plot show the switching of the JJs. This plot has several I-V curves superimposed one over the other due to the property of the fast-sampling scope. The switching moment changes when a crude aluminium foil shield is put over the connection box. It was observed that the extent of noise changes from time to time, and better results were observed at late hours after switching-off the wireless network on the floor where the laboratory is located.

These experiments were carried out for different JJ chains and chips to make sure that a particular JJ chain is not having the specified problem. After these (very time consuming – several hours including preparation) experiments it was decided that a noise-free environment is essential for this sensitive low-temperature measurements involving several hundreds of JJs at a time to derive any useful results from these chips.

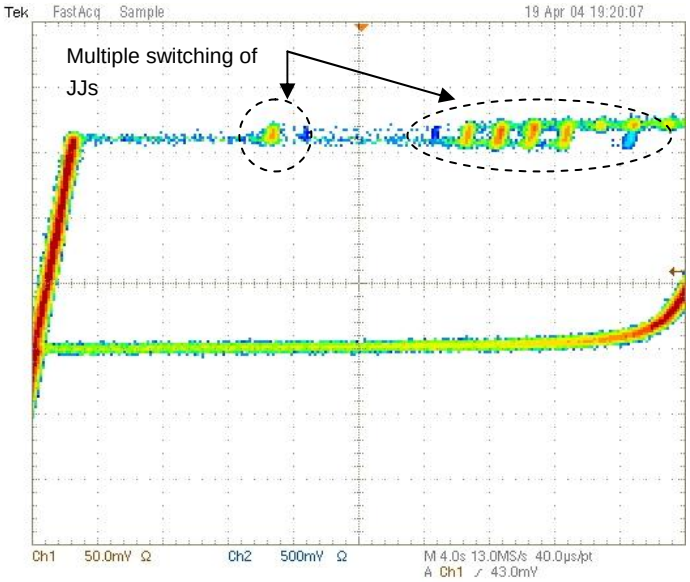

Figure 5.24: An enlarged portion of the I-V curve using a Tektronix fast-sampling scope showing the noise-induced switching of a JJ chain; it is concluded to be resulting from the background noise in the laboratory.

A new setup was prepared for repeating the experiments in a shielded room (Faraday cage) to verify the earlier claims. A mini-cryostat that was available in the LT laboratory was used as a dewar for these experiments. A trial probe was constructed for the mini-cryostat as this cryostat was sufficient for these trial experiments. A new connection box was also prepared which is much simpler in nature for this verification experiment. If fully filled, the cryostat can hold the test chip at 4 K for 2-3 hours. Due to the limitation of the special sealed-connector fixed on the connection box, only 6 copper wires were available for this probe. This limited amount of available wires reduced the number of different JJ chains that could be connected and measured by the experimental setup to two. No I_c-B experiments were planned using this small cryostat and hence no superconducting coil was used in this set-up. The available power supply for SQUID measurements as mentioned before was used here also. The simplified wiring schematic is shown in Figure 5.25, which is a straight-forward 4-point measurement for the JJ chains. The mini-cryostat with the connection box was placed inside the shielded room. The connections were made to the SQUID electronics using shielded cables.

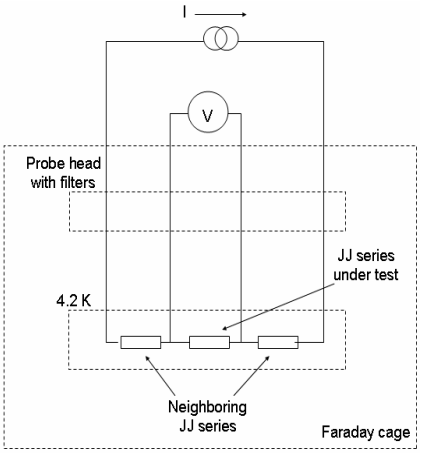

Figure 5.25: The modified experimental schematic for I-V measurements on the JJ chains in the test chips (see text for details).

This temporary setup was prepared in order to verify the concept before adapting it to a new (expensive) LT setup with more connection wires and features or alternatively equipping the LT lab with a Faraday cage. Hence, the results from these experiments remain qualitative in nature. Further detailed measurements are required before presenting any quantitative results. This was due to a lack of available time. These experiments were carried out in the shielded room in the Bio-magnetic Centrum Twente (BCT) to avoid the external noise which hampered the previous experiments.

Figure 5.26 shows an example measurement plot obtained at the BCT. The results are from a good series of JJs as measured before. When the JJ chains were measured, at first there were multiple switching as in the case of earlier experiments. This was due to the fact that the JJs were cooled from RT to 4 K and the probability of flux trapping is always higher in this case as mentioned before. But, on recooling the multiple switching disappeared and the JJs switched at the same instance. So it was clear that the dotted line shows the measurement while some flux-trapping occurred in the JJs. This resembles the plots obtained earlier verifying that the cause of the multiple switching earlier was due to flux trapping in a noise field. The solid line shows a re-plot of the same series after a second cooling step. Now, all the JJs switched at the same time showing the good series of JJs.

As mentioned before, this recooling technique is used to avoid trapping of magnetic flux in the JJs while cooling from RT. In the case of earlier experiments, this recooling technique did not work very well. Due to the background noise in the lab, there was always flux trapping.

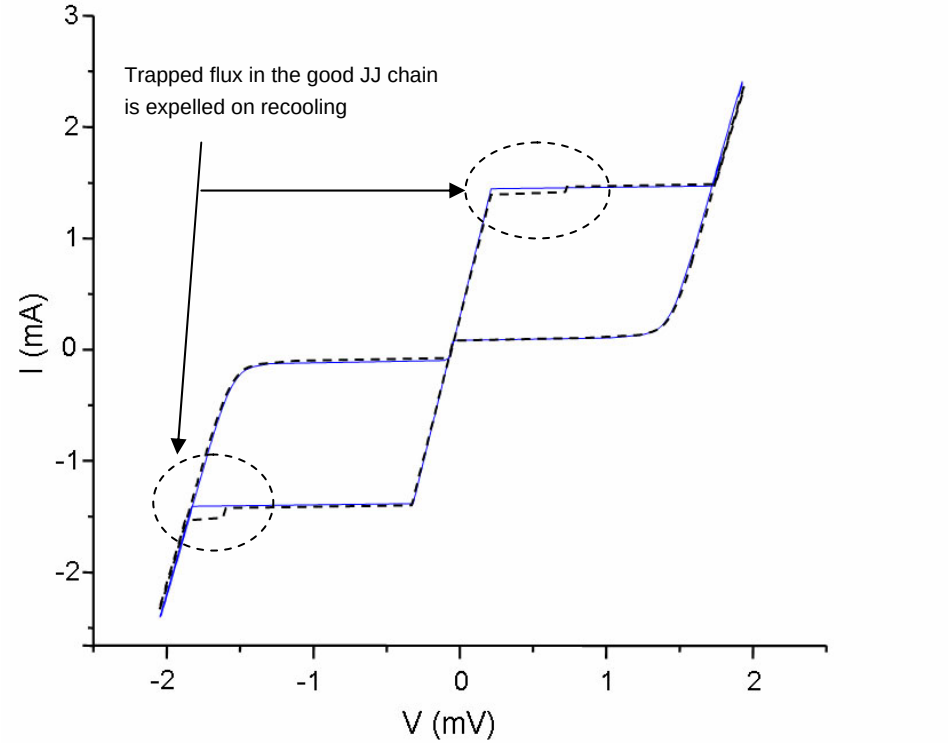

Figure 5.26: I-V plots of a series of good JJs. The dotted line shows the plot with multiple switching of JJs due to flux trapping and the solid line plots the correct I-V curve after recooling (scale in arbitrary units).

In the next step, the experiments were repeated with defect-induced JJs. Figure 5.27 and Figure 5.28 show the behavior of a defective series. The plot shows one complete cycle of an I-V curve. As mentioned in the previous chapter, these are the results from deliberately designed defect-induced series.

Figure 5.27 shows the result from a series in which a defect induced JJ is present. In this case, a short was induced in one of the JJs. The critical current of a junction has reduced as expected by the early switching of the JJ as explained in Chapter 3 and reference [1]. The situation did not change even after repeated recooling. The switching instance was always the same throughout the experiments. This shows that the multiple switching is caused by the defect-induced JJ.

Figure 5.28 shows the result from a series in which the induced defect is an open in a JJ. An irregular step height and leaky return current is observed in a JJ due to the induced defect as the plot remains the same after repeated measurements and recooling. This indicates the possibility to detect the defect as explained in Chapter 3 and reference [1]. This behaviour of an open JJ is not fully understood yet and needs further investigations. It

could also be due to the non-ideal design of an open as presented in Chapter 4 of this thesis.

All plots presented in this section are in arbitrary units and shown to prove that our concept is correct for a structure to detect a defective JJ in a series of JJs. The deliberately induced defective JJs were distinguishable in a series of JJs as shown in Figure 5.27 and Figure 5.28. Hence, if a JJ happens to be defective, its presence can be detected by the above structure and measurements.

This shows that the fault-modeling approach is also correct for a shorted JJ, since the critical current is reduced for such a JJ. More details on fault-modelling are presented in Chapter 6 of this thesis. This has to be verified by the experiment presented in Chapter 6 of this thesis. In the case of an open JJ, more investigations are required before arriving at such a conclusion. This is due to the facts further discussed in the fault-modeling part of Chapter 6 of this thesis as well as the non-ideal nature of the deliberately induced open in a JJ as described in Chapter 4 of this thesis. Further experiments have to be carried out as mentioned before and will be the next step regarding this work to provide quantitative results on defect statistics. This has not been carried out due to a lack of time.

Since the low-temperature measurements have proven to be extremely time consuming, the original idea to bring about all the measurements at room temperature is very relevant. Currently, only an indication that the proposed approach is sufficient for the detection of defects is available from the presented experiments as they remain qualitative in nature. An efficient measurement system has to be developed as the described set-up was for experimental purposes only. The defect behavior has still to be translated to room-temperature values to provide useful statistics using quantitative data using an efficient measurement system. The structures are designed so that this is possible, but this is a very time-consuming process and is the next step that has to be carried out in the future.

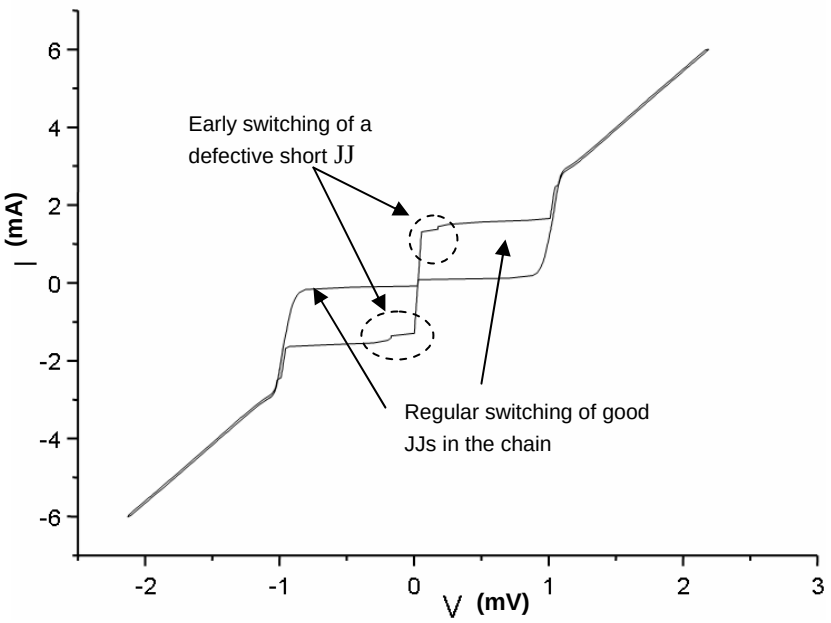

Figure 5.27: I-V plots of a series of JJs with a deliberately induced defect showing the capability of the proposed setup for detection of defects in a series of JJs. Here the induced defect is a short in a JJ (scale in arbitrary units).

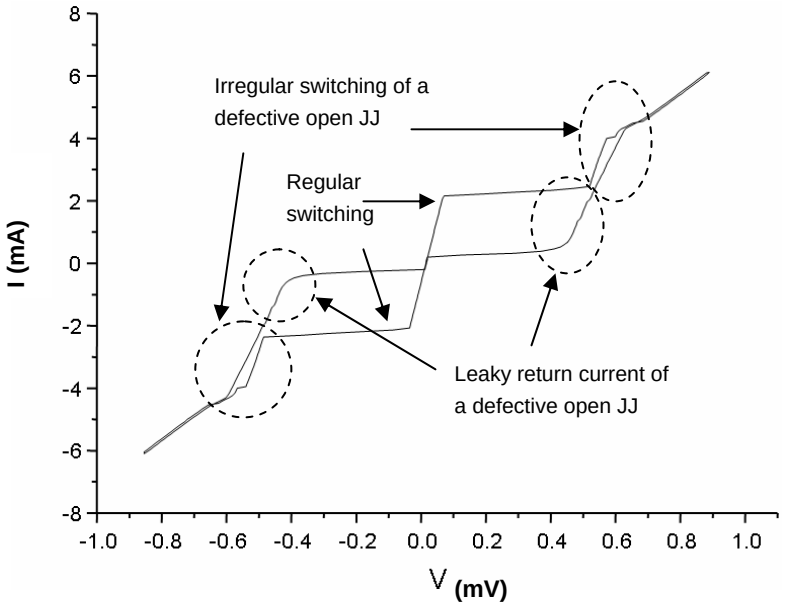

Figure 5.28: I-V plots of a series of JJs with a deliberately induced defect showing the capability of the proposed set-up for differentiating a defect. Here the defect is an open in a JJ (scale in arbitrary units).

5.6 Conclusions

Measurement results from our designed test chips developed for the two investigated RSFQ processes have been presented in this chapter. A quantitative data analysis has been performed on the room-temperature structures while a qualitative approach on low-temperature structures showed that the proposed approach is suitable for a quantitative analysis in the future.

Since ten chips per wafer were available from the JeSEF process, a detailed wafer mapping could be performed. Since it was a less mature process than the HYPRES process, less number of different test structures were implemented. The statistical information from the developed test-structures proved that they are capable of extracting defect information for SCE circuits being processed at JeSEF.

The HYPRES process was extensively analysed by implementing different types of test structures. Only three test chips were available per wafer in the HYPRES process. Hence the results were limited. The foundry upgrade and renovations at HYPRES have affected the statistics by increasing the probable defects. A ranking list was prepared from the 25 different structures. Since the HYPRES process has been modified, also taking into considerations the results from this investigation, a new ranking list has to be prepared after another investigation and this is clearly future work.

From both processes it was concluded that the step-coverage at the via interconnects pose a significant problem. Information about yield in both processes can be derived from these results by applying these values to a suitable yield model. This information will also be useful for inductive fault analysis while developing an ATPG approach for RSFQ circuits.

Experimental set-up for the detection of defects in a JJ at 4 K has also been presented in this chapter. It was found that the LT measurements are extremely time-consuming and very sensitive to noise. It was also showed that a shielded room (Faraday cage) is required for carrying out the described experiments. It was shown that the proposed approach is sufficient for the detection of defects in a JJ if a shielded room is available. It was shown that the fault-modelling approach in the case of a shorted JJ is correct. More detailed research has to be carried out for correlating the LT measurements to RT measurements.

5.7 References

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Chapter 6

Defect-Based Testing of LTS RSFQ Circuits

This chapter deals with the methodologies applied to the testing of RSFQ circuits. The development of fault models for RSFQ circuit testing is covered in this chapter based on the results from the developed test-structures. Two defect-based test (DBT) methodologies are enumerated in this chapter. The preliminary investigation led to a detailed study of an RSFQ D-type flip-flop (DFF). Test chips were developed incorporating defect-induced DFFs to study the actual behaviour if probable defects are present in the realized circuit. The chapter concludes with the design implementation of test chips which will be used for the verification of the developed fault models in the future.

6.1 Introduction

The ultimate goal of this research work is to develop Automatic Test Pattern Generation (ATPG) for SCE logic circuits. Investigating the possibility of whether or not the available ATPG techniques are applicable is one of the major concerns in the process. Otherwise new ATPG techniques have to be developed for SCE. As mentioned in Chapter 4, information about defects and their subsequent translation into fault models are crucial at this stage. Test structures as presented in Chapter 4 are used to gather information about defects in this process. The defect information presented in Chapter 5 is subsequently used for Inductive Fault Analysis (IFA). The behaviour of the defects is predicted from this gathered information and fault models are proposed accordingly. This chapter deals with the development of fault-models for RSFQ circuits. The organisation of the chapter is as follows.

As mentioned in the earlier chapters, a defect is a deviation of the physical parameters beyond the tolerance limits of the structures of an IC from the properties predicted by its design. A fault is defined as a defect that causes the results of the electrical measurements of the IC structure to differ from required parameters resulting in malfunction. The process of translation of a physical defect into suitable electrical values, so that its presence can be predicted using circuit simulation, is known as fault-modelling.

Section 6.2 deals with the investigation carried out for the Defect-Based testing (DBT) of RSFQ circuits. Some of the early works on the topic are also mentioned in this section. Further research was carried out on an RSFQ DFF circuit with the preliminary measurement results from the JeSEF process presented in Chapter 5. Section 6.3 presents the details of this work in which a transient current testing method for an RSFQ circuit has been carried out for the first time. Fault models for RSFQ circuits are proposed and a detailed investigation is required to verify the correctness of the chosen approach.

As the JeSEF process was not adequate for realising complex circuits, the HYPRES process which is more mature had to be used for this purpose. Sections 6.4, 6.5 and 6.6 present the details of this work.

In Section 6.7, the Design-for-Test (DfT) methodology presented in Chapter 3 of this thesis is applied for the verification of the developed fault models.

6.2 Early work on RSFQ circuit testing

As mentioned in the third chapter of this thesis, the test approaches prevailing for RSFQ circuits are functional in nature. The research reported in this thesis accounts for the structural testing approach for an RSFQ circuit. Some of the earlier works on this subject are reported in references [1] - [3]. These were pure theoretical work based on information mainly available from semiconductors. A defect in a Josephson Junction (JJ) was modelled as a 10 times change (increase or decrease) in the normal I_c value. Opens were treated as complete opens, bridges as 1 fΩ resistances, a bad contact resistance as 100 Ω between a resistor and a superconductor, and 0.1 Ω between two superconductors. It was also

predicted pre-maturely, as there were no defect data available, that the stuck-at-fault model approach is applicable in the case of RSFQ circuits. Power-supply current monitoring was also carried out by grounding all the inputs and outputs while the supply voltage is swept from 0-20 mV.

This information, along with the measurement results on the Process Defect Monitors (PDM) developed for the processes, were used in this research to develop detailed models as well as concrete data on the translation of defects. The first experiments were carried out on a flux amplifier / flux multiplier, which is one of the elements in an SCE ADC [4], [5]. This flux multiplier is shown in Figure 6.1. It consists of an SFQ splitter and a confluence buffer [6] . With the pulse splitter, SFQ pulses are replicated. The confluence buffer combines them, resulting in the effect of multiplication. A delay is introduced between the pulses so that they will not reach the confluence buffer at the same time; in this case only one SFQ pulse will be available at the output. In the scheme, JJs are indicated as "X", I_b is the biasing current and "D" a delay block.

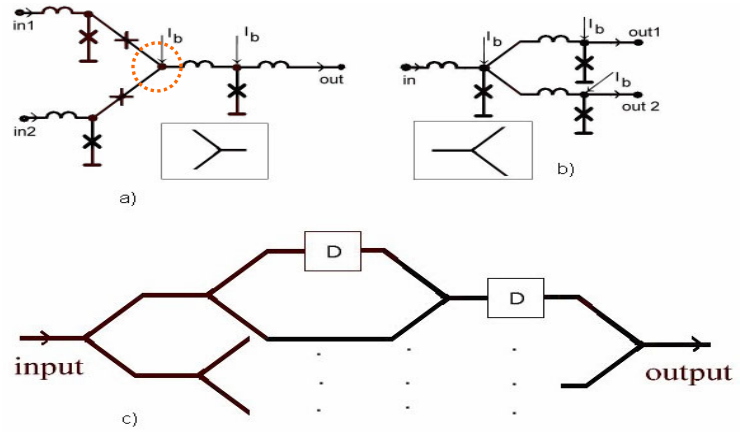

Figure 6.1: a) Schematic and symbol of a confluence buffer and b) an RSFQ splitter. c) Circuit schematic for a flux multiplier. The assumed defect location is a via in the confluence buffer and is marked by the dotted circle.

The experiments were carried out using JSIM [7] – a Spice variant for RSFQ circuits. This was developed at UC Berkeley and was adapted for the PC platform and enhanced with a waveform viewer at the University of Twente. A defect is assumed at the node connecting the two branches of the confluence buffer, shown by the dotted circle (Figure 6.1a). At this node, an M2-M1 via is present to connect the two M1 lines of the branch to the M2 line of the output JJ. The resulting outputs are shown in Figure 6.2. Figure 6.2a shows the correct operation of the flux multiplier. Figure 6.2b illustrates the faulty operation if the above mentioned defect was induced. This work has been presented in detail in [8].

The fault was induced by inserting a resistance of 60 mΩ in the netlist of the amplifier at the marked location in Figure 6.1a. This value for the defect was found by extensive simulation experiments and it showed that if the resistance of a via is above 60 mΩ it becomes defective in nature. As flux-multiplier, being an asynchronous circuit is too complex to be used for establishing the proposed ideas, the investigations were focused on one of the simplest synchronous logic circuits in SCE, being a D-type flip-flop. As the primary focus of the research was towards the JeSEF process, further investigations were carried out on a DFF designed in the JeSEF process.

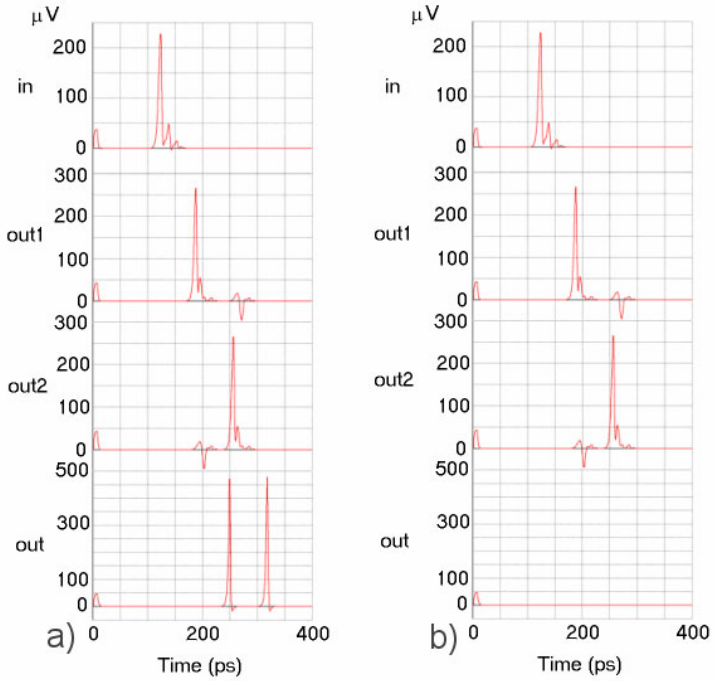

Figure 6.2: Output of a simple flux multiplier. a) Correct operation b) Faulty behaviour if one of the vias is defective.

6.3 Experiments on a JeSEF DFF

To illustrate the DBT approach, a D-type Flip-Flop (DFF) designed in the JeSEF process is considered as an example. The RSFQ circuit schematic of the DFF is shown in Figure 6.3. This is the same DFF circuit as described in chapter 3 of this thesis. A superconducting loop is formed by J2-L2-J3 where the data will be stored as a fluxon. As mentioned in the previous chapters, inductances are implemented using the metal wiring layer. The buffers made of JTLs before the inputs and after the outputs in an actual implementation are not shown in Figure 6.3 for the sake of simplicity.

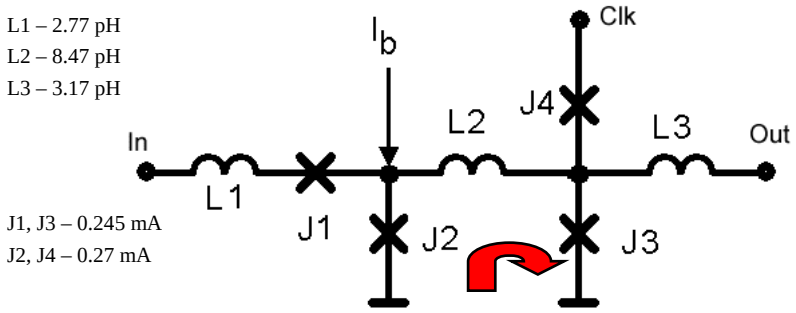

Figure 6.3: Circuit scheme of an RSFQ D-type Flip-Flop.

In order to study the influence of the defects in the JeSEF process, a DBT strategy was applied to this DFF designed in the process. This was carried out under the condition of a maximum operating frequency of 17 GHz at 4.2 K [9]. Both current as well as logic-based testing approaches were carried out to gain a better understanding of the test methodology that should be used in SCE circuits. The induced faults are resistive in nature. The information gathered from the earlier studies on the faulty behaviour of RSFQ circuits was used in the experiments. It was found that an introduction of 0.6 Ω was sufficient for the complete malfunctioning of the circuit. It was also observed that the circuits start misbehaving, even if the value of the induced resistor is as low as 60 mΩ. This is due to the fact that RSFQ circuits work in the super-conducting state. For the simulation experiments

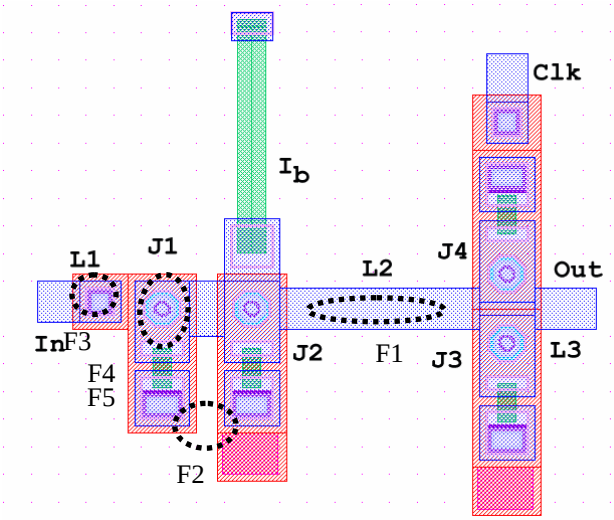

Figure 6.4: Layout of a DFF in the JeSEF process. The dotted circles show the location of the insertion of defects in the circuit as explained in the text.

described in this section, each time the *minimum* resistance that was able to produce a detectable faulty behaviour was introduced in the circuit and the corresponding currents were observed.

A simple layout of the DFF is given in Figure 6.4. The locations of the introduced faults in the netlist are marked by ellipses. The first fault to be introduced is a crack in the storage inductor L2, denoted by "F1". In this case a 0.5 Ω resistor was introduced. The next fault (F2) that was considered is a short in the node connecting J1 and J2 to ground. This is possible if a short is present between the M1 layers of the grounded and the un-grounded junction, connecting the above-mentioned node to ground. In this case a 0.43 Ω resistor was introduced in the netlist.

The third fault (F3) that has been introduced is resulting from the M1-M2 via problem and a 0.6 Ω resistor was introduced in this case. The next 8 faults (F4-F11: only shown for J1 in Figure 6.4, F4 and F5, for simplicity) were shorts and opens in the thin Al_2O_3 barrier of the 4 JJs present in the circuit. In the case of a short, a 0.1 Ω resistor was introduced in parallel to the JJ and a 100 Ω resistor was introduced in the JSIM model of the JJ, as described in chapter 2, for the open case. The details of the simulations are given in the following subsections.

6.3.1 I_{DDX} Testing

Current testing is an effective methodology in full CMOS semiconductor circuits to analyse defects. I_{DDQ} is a test technique based on measuring the current of the device under test [10], [11]. However, I_{DDQ} test does not detect defects which do not produce sufficient increase of the quiescent current and defects producing exclusive changes in the dynamic current are not I_{DDQ} testable [12]. On the other hand I_{DDT} test methodology, tries to overcome the limitations by measuring the transient current in the circuit [13]. I_{DDT} testing has not yet been applied to SCE circuits. An I-V measurement is used to characterize a JJ as mentioned in one of the previous chapters. As a JJ is a current-controlled device, a current-based testing technique seems attractive. The fact that the currents involved are very small in magnitude, as well as the lack of a systematic test methodology in SCE, is the reason that current testing was not yet implemented. The observation methodology presented in chapter 3 of this thesis can also be used in the implementation of current testing. The current flowing through output inductor L3 (Figure 6.3) was monitored during the simulations. This can be implemented by inductively coupling L3 with another inductor connected to an SCE amplifier. Eleven faults in the DFF as described in section 6.3 were detected by simulation using the I_{DDT} technique. Different open and shorts were introduced into the circuit netlist for the experiments.

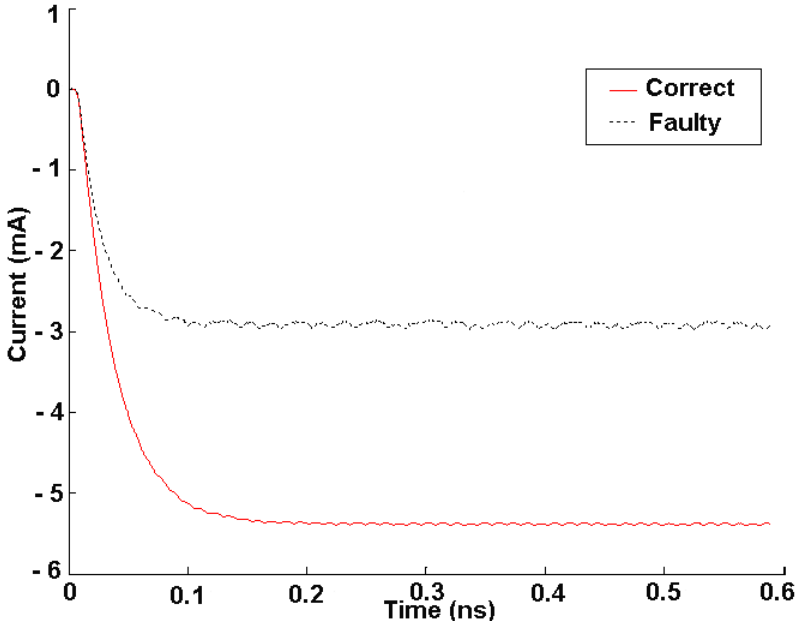

Figure 6.5: Defect detection in a DFF using the I_{DDT} testing technique. The assumed defect is a crack in the storage inductor L2 (F1).

These simulations were carried out using JSIM [7] and the resulting data was analysed using MATLAB. One of the plot results of the transient current-testing approach is given in Figure 6.5. The assumed defect is a crack in the storage inductor L2 (F1). It shows that the defect is detectable using this technique. Note that the currents are small in magnitude, in the order of a few mA, but compared to the current in a defect-free circuit, about 50% change in value was observed. Defects resulting in less than 25% deviations were considered to be undetectable. This is set to this value such that because of the allowed 20% design margins in an RSFQ circuit. While performing the simulations, the normal input signal was replaced by a constant voltage source.

6.3.2 Digital Structural Testing

As mentioned before, a functional test is commonly used in SCE for the hardware verification of the design implementation. Figure 6.6 shows the correct functional operation of the previously discussed DFF. A digital structural test technique was applied here. The same 11 faults described before in section 6.3 were used in this digital test approach for comparison with current-based testing. Similar approaches as discussed in [8] were used for analysis. The following functional errors were observed during simulations:

a) The input signals were influenced by the defect and resulted in incorrect operation

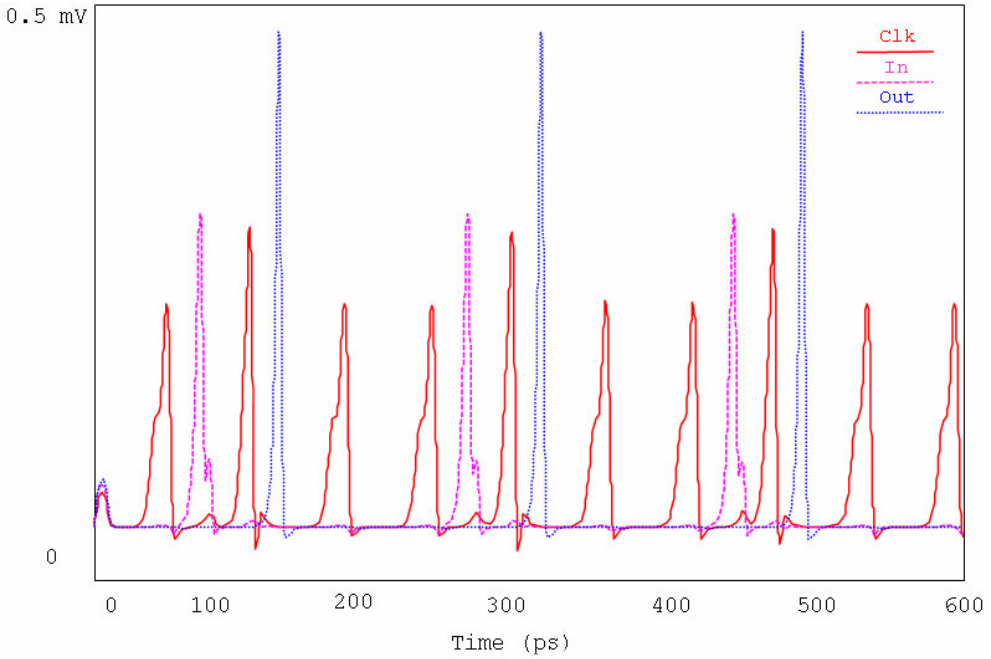

Figure 6.6: Simulation of the fault-free operation of an RSFQ DFF.

b) The output signals were delayed for a certain period depending on the severity of the fault

c) No response resulted from the output ports.

In other cases, the input or output signals were slightly distorted, but the logic operations were not affected making such defects undetectable using digital structural testing. The test results are now discussed in detail. In all cases, the same test vectors were used, exhaustive test due to the simplicity of the circuit. Figure 6.7 shows the case ‘a’ as explained above. Case ‘a’ was observed if the second fault (F2), i.e. the JJ nodes connecting J1 and J2 shorted to ground as mentioned in the previous sub-section, was introduced. A resistive bridging was used in this case as described in Section 6.3.

Case ‘b’ was observed if the assumed defect was a crack in L2 (F1). The resulting output is as shown in Figure 6.8. The delay is 6 clock cycles as can be observed in this case.

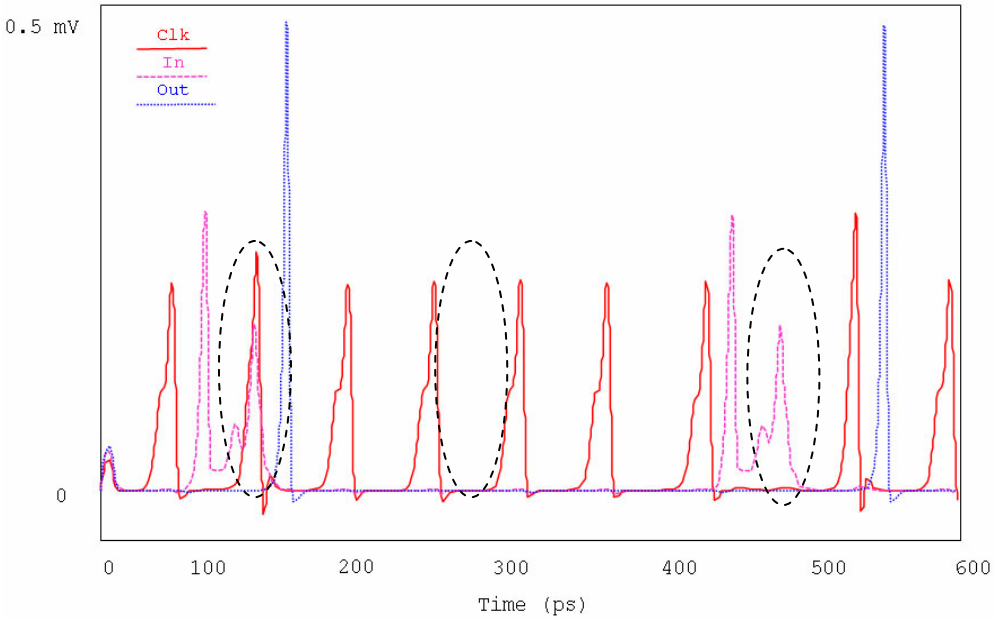

Figure 6.7: Defect detection using digital structural testing: case a) the input signals are being influenced by the defect resulting in faulty operation (marked by ellipses). The assumed defect is a node shorted to ground (F2) using a resistive bridging fault model (see Section 6.3).

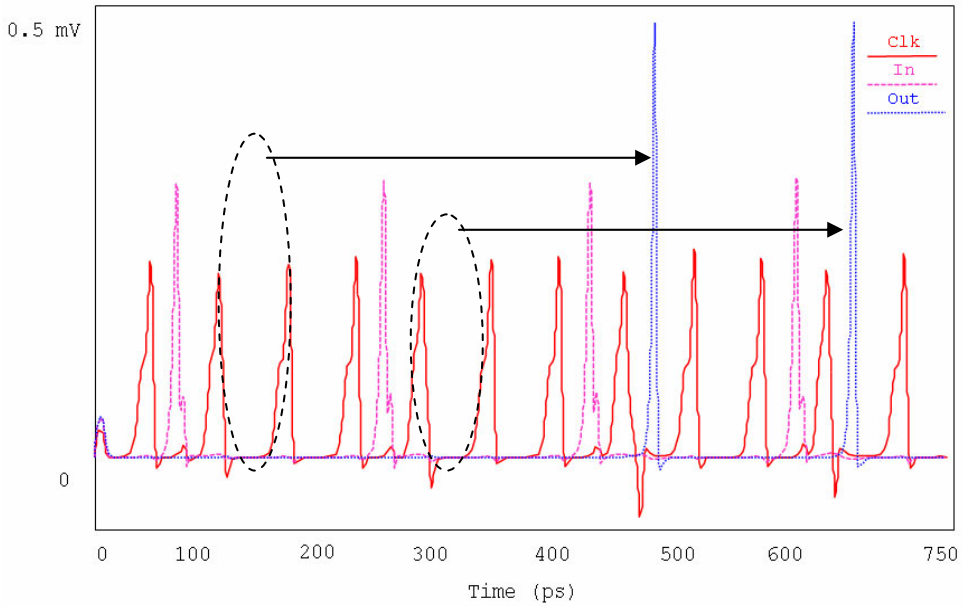

Figure 6.8: Defect detection using digital structural testing: case (b) output signals are delayed for a certain period (the ellipses show the location of the expected pulse). The assumed defect is an open in the storage inductor L2 (F1 - Section 6.3).

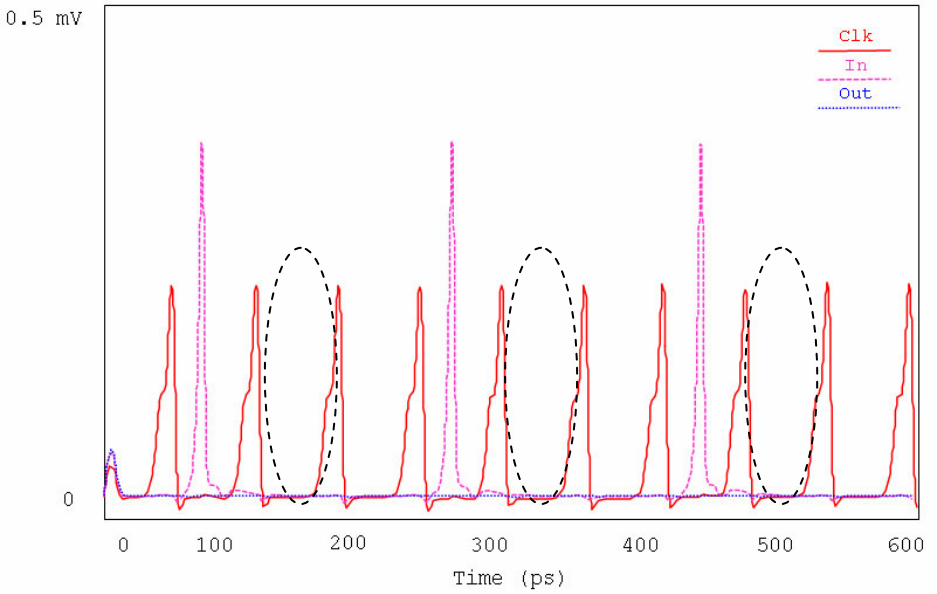

Figure 6.9: Defect detection using digital structural testing: case (c) no response from the output port (marked by ellipses). The assumed defect is an open in a via (F3 - Section 6.3).

By introducing the M1-M2 via fault (F3), case 'c' was observed and this is shown in Figure 6.9.

The SFQ pulses are of very small magnitude (up to a mV). They have to be amplified using SCE amplifiers before applying them to conventional test equipment.

The results of the previous simulations are given in Table 6.1. The second main-column provides the details of the faults induced and is divided into three sub-columns. The first sub-column shows the induced faults while the detected and un-detected faults are given in the second and the third sub-columns. These opens and shorts were introduced in the JJs, interconnects and vias. The reason for some of the defects in one section (for e.g. input) of

Table 6.1: Two different testing approaches of an RSFQ DFF

DFF Testing	Induced Faults		Detected		Undetected	
	Open	Short	Open	Short	Open	Short
Current-based testing	6	5	2	3	4	2
Digital structural testing	6	5	4	5	2	0

the circuit that affects the functionality of others (e.g. clock), is that SCE circuits operate in a super-conducting state. A defect in one of the elements in the super-conducting loop influences the other element and is in many cases indistinguishable due to the magnetic flux-quantum behaviour. A comparison of the test results was carried out with respect to digital structural and I_{DDT} testing.

From these preliminary results, shorts or bridges seem easy to detect while opens tend to escape the test. All the introduced shorts could be detected by digital structural testing. This could again be a result of super-conducting loops: – new loops are formed if a short occurs which changes the behaviour of the circuit. From the initial results, it may be assumed that I_{DDT} testing does not provide more information as compared to digital structural testing in the case of SCE circuits, since all the I_{DDT} detected defects were already detected by digital structural test, contrary to that in the case of silicon semiconductor circuits. But, it was concluded that a more detailed study has to be carried out to verify these arguments as the available information is limited. Even though fewer defects were detected using a current testing approach, a more detailed study is required before making general conclusions.

From the measurement results presented in chapter 5 of this thesis, it has become clear that the JeSEF process will probably not be able to handle the necessary complexity for a realisation of a test chip required to carry out the studies mentioned in this section. As a result, the HYPRES process was chosen for further study in this matter.

L1 = 2.74 pH
L2 = 6.075 pH
L3 = 1.975 pH
L4 = 1.064 pH
J0 = 0.2375 mA
J1 = 0.2375 mA
J2 = 0.185 mA
I_b = 0.125 mA

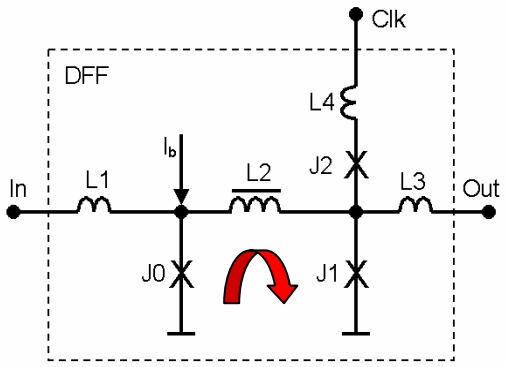

Figure 6.10: Schematic with optimised circuit parameters of the RSFQ DFF designed in the HYPRES technology which will be used as CUT.

6.4 Defect-Based Testing of a HYPRES DFF

Information from the Process Defect Monitor (PDM) test-chip developed for the HYPRES process as described in chapters 3 and 4 of this thesis helped to identify the probable defects in the DFF layout. The defect ranking list based on the experimental results presented in Chapter 5 is given in Table 6.2. The first column defines the rank of the particular defect mentioned in the second column.

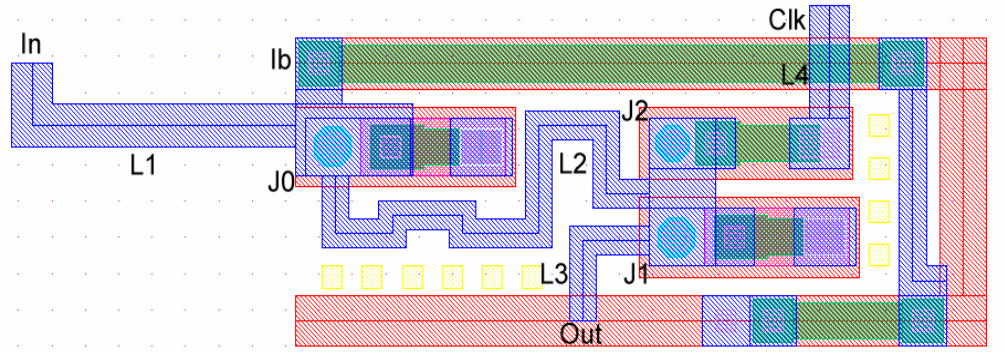

Figure 6.11: CADENCE Virtuoso layout of an RSFQ DFF designed in the HYPRES Nb process. The M3 layer is used as second ground plane and is not shown for clarity.

Table 6.2: Ranking of the defect-prone areas in the HYPRES process.

Rank #	Resulting Defect
1	M3 crack over an M3M1 via
2	M3 crack over an M3M2 via
3	M3 crack over an M3M0 via
4	Crack in M3 over an M2 edge
5	Crack in M3 over an M2 edge
6	Crack in M3 over an M2M1 edge
7	Crack in M3 over an M2 edge
8	Short between M3 & M2 over M2 edge
9	Short between M3 & M2 over M2M1 edge
10	M2 crack over an M1M0 via
11	M2 crack over an M2M0 via
12	M1 crack over an M1M0 via
13	Crack in M2 over an M1 edge
14	M2 crack over an M2M1via
15	M2 crack over a 2μ M2M1 via
16	Short between M2 & M1 over M1 edge
17	Short between M2 & R2 over R2 edge

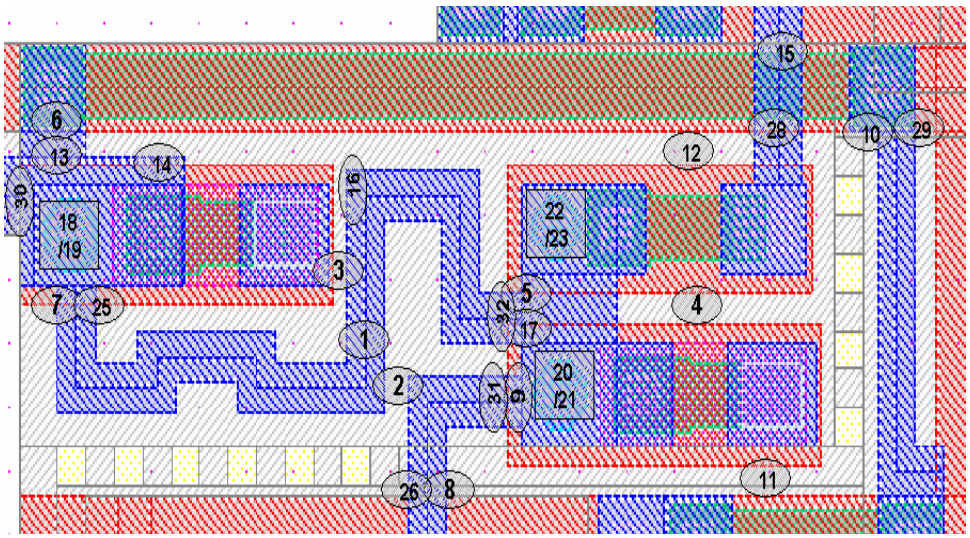

Figure 6.12: Part of the (magnified) layout of a HYPRES DFF showing the defect-prone locations in the cell. These locations were used to induce deliberate defects.

This information along with the topography of the layout was used to determine the defect-prone locations in the layout. Wiring and interconnect defects, like vias, are the main concerns for this matured fabrication process since the layouts are more dense in a commercial process. The usage of the second ground plane increases the probability of random defects even though it increases circuit stability and margins. This is due to the fact that one more conducting layer is involved in fabrication.

Figure 6.10 shows the circuit schematic of a DFF designed in the HYPRES process. The corresponding layout in this process is shown in Figure 6.11. Details of this circuit were presented in chapter 2 of this thesis. The ranking presented in Table 6.2 is resulting from the structural analysis of the HYPRES process presented in chapter 5. This table looks different from Table 5.7 as this is from the circuit designers point of view (not taking into account the layout details like wire-width). As mentioned in chapter 3, defect-prone areas do not necessarily mean defect-prone locations in a circuit. Only those locations where critical areas are involved results in a defect-prone location in a layout. Thirty-two defect-prone locations in the HYPRES DFF layout were identified. Since M2 crosses many other layers and is used for extensive wiring and for realising inductors, the majority of the defects were related to this layer. Twenty-three of the identified defect locations involve M2, where shorts and opens are the major concerns. M1 and M3 follow in the number of locations and six defect locations are related to JJs.

Part of the defect-prone locations in the DFF layout is shown in Figure 6.12. The central section of the DFF layout is magnified to show the details. Since L2 is the longest wiring having several bendings/edges, there is a higher probability for a crack/open in the inductor. This is shown by (1) in the layout of Figure 6.12. An intra-layer short in M2 (2), bridging L2 with L3 is also quite probable, since they are at minimum required separation

according to the design rules. The complete list of identified locations is given in Table 6.3. Details are explained in the next sub-section.

6.5 The Modelling of Defects

Modelling the most probable defects in the circuit was the next step involved in the test flow. Knowledge gained from the earlier work as presented in the previous sections was used for the modelling of defects in the SCE circuit. Table 6.3 gives the details of all defects that have been investigated, their location as well as the model used. The first column shows the reference number in the layout (Figure 6.12) where the locations of the defects are shown. The second and the third columns enumerate the type of defect at a particular location. The notation refers to the names of schematic elements in Figure 6.10 and its layout in Figure 6.11. The results of the defects in the circuit are given in the fourth column and the used modelling in the last column.

The resistance values for shorts are in accordance with the contact resistance of the metal, e.g. metal-metal or metal-resistor, in its superconducting state. The value (0.65 Ω) of resistance for a crack/open is also resulting from the previous study.

The fault models for defective JJs are modifications of the corresponding JJ model [14] in JSIM (see chapter 2 of this thesis on JJ models) being used for the simulation of RSFQ circuits.

Table 6.3: Details of the defect-prone locations and modeling of those defects in the DFF circuit.

Number	Type of Defect	Location	Result of Defect	Used Model
1	M2 crack/open	@L2	L2 cracked or open	Resistance of 0.65 Ω
2	M2 short	Between L2 & L3	L2 shorted to L3	Resistance of 1 mΩ
3	M2 short	Between L2 & J0	L2 shorted to Gnd	
4	M1 short	Between J1 & J2	Clk and Gnd shorted	
5	M2-M1 short	@J2	Clk & L2 shorted	Resistance of 0.1 Ω
6	M2-M1 short	@I_b	L1 shorted to bias line	
7	M2-M1 short	@J0	L2 shorted to Gnd	
8	M2-M1 short	@Out line	Out shorted to Bias line	
9	M2-M1 short	@J1	L3 shorted to Gnd	
10	M3-M2 short	@Middle of I_b	Bias line shorted to Gnd	
11	M1 short	Between J1 & bias line	Bias line shorted to Gnd	Resistance of 1 mΩ
12	M1 short	Between J2 & bias line	Bias shorted to Clk	
13	M2-M1 short	@J0	In shorted to Gnd	Resistance of 0.1 Ω
14	M3-M2 short	@J0	In shorted to Gnd	
15	M2-R2 short	@Clk line	Bias line shorted to Clk	
16	M3-M2 short	@L2	L2 shorted to Gnd	
17	M2-M1 short	@J1	L2 shorted to Gnd	
18	Tri-layer short	@J0	Shorted J0	R_0 = 10 mΩ
19	Tri-layer open	@J0	Open J0	R_0 =100 kΩ
20	Tri-layer short	@J1	Shorted J1	R_0 = 10 mΩ
21	Tri-layer open	@J1	Open J1	R_0 =100 kΩ
22	Tri-layer short	@J2	Shorted J2	R_0 = 10 mΩ
23	Tri-layer open	@J2	Open J2	R_0 =100 kΩ
24	M2-M1 short	@In line	In shorted to bias line	R of 0.1 Ω
25	M2 crack/open	@J0	Cracked/Open L2	Resistance of 0.65 Ω
26	M2 crack/open	@Out line	Cracked/Open L3	
27	M2 crack/open	@In line	Cracked/Open L1	
28	M2 crack/open	@Clk line	Cracked/Open L4	
29	M2 crack/open	@Middle of I_b	Crack/Open in bias line	
30	M2 crack/open	@J0	Cracked/Open L1	
31	M2 crack/open	@J1	Cracked/Open L3	
32	M2 crack/open	@J2	Cracked/Open L2	

This modification and justification is now discussed in detail. Each JJ has a subgap-resistance value denoted by R_0 as well as a normal-state resistance denoted by R_N in the model (see Chapter 2 of this thesis). The R_0 value of a good JJ for the HYPRES Nb process is in the order of 100 Ω [15] and the R_N is of the order of few Ohms. In the case of a short in a JJ, which can be considered as a result of a large pinhole, the thin Al_2O_3 barrier is penetrated by a contact electrode. The normal state resistance of the JJ is thereby reduced to the contact resistance of a superconducting wire. This is modelled as a 10 mΩ resistance due to the very thin barrier separating the superconductors [16].

In the case of an open in a JJ, for e.g. due to the presence of a foreign particle in the trilayer, the (defective) R_N value will be much higher than its normal value. This value for R_N can vary from a few Ohms to mega Ohms in case of a complete open. This was modelled by 100 kΩ resistors. This is due to the fact that the dynamic resistance of a JJ (see Chapter 3 of this thesis) is in the order of kΩ [15]. However, a resistance of few ohms is already sufficient for a faulty behaviour of the DFF. Due to this, the junction capacitance and the critical currents of the JJ will also reduce as a result of the decrease in the junction area of the defective JJ. This reduction has been set as 20% due to the circuit margins mentioned earlier even though a few percentage is enough to cause faulty behaviour in a defective JJ.

Simple yet accurate models which can describe the faulty behaviour of the circuit was one of the primary concerns in this chapter. The following lists a summary of the fault models that were used for JSIM simulations of the DFF HYPRES circuit.

• A crack/open in a superconductor metal layer is modelled by a resistor of 0.65 Ω

• An intra-layer short in a superconductor metal layer is modelled by a resistor of 1 mΩ

• An inter-layer short between two superconducting layers is modelled by a resistor of 0.1 Ω

• An inter-layer short between a superconductor layer and the resistor layer is modelled by a resistor of 0.1 Ω

• A short in a JJ is modelled by a resistor of 10 mΩ as the R_0 and R_N values of the JJ model as well as a reduction in the junction I_C value by 20% in the JSIM model

• An open in a JJ is modelled by a resistor of 100 kΩ as the R_N of the defective JJ as well as a reduction in the junction capacitance and the I_C values in the JSIM model by 20%.

Extensive simulations were carried out inducing these defects using the described fault models and introducing them in the circuit netlist. The used fault models were inserted at the appropriate location in the netlist of the HYPRES DFF. The details of these simulations will be discussed in the next section.

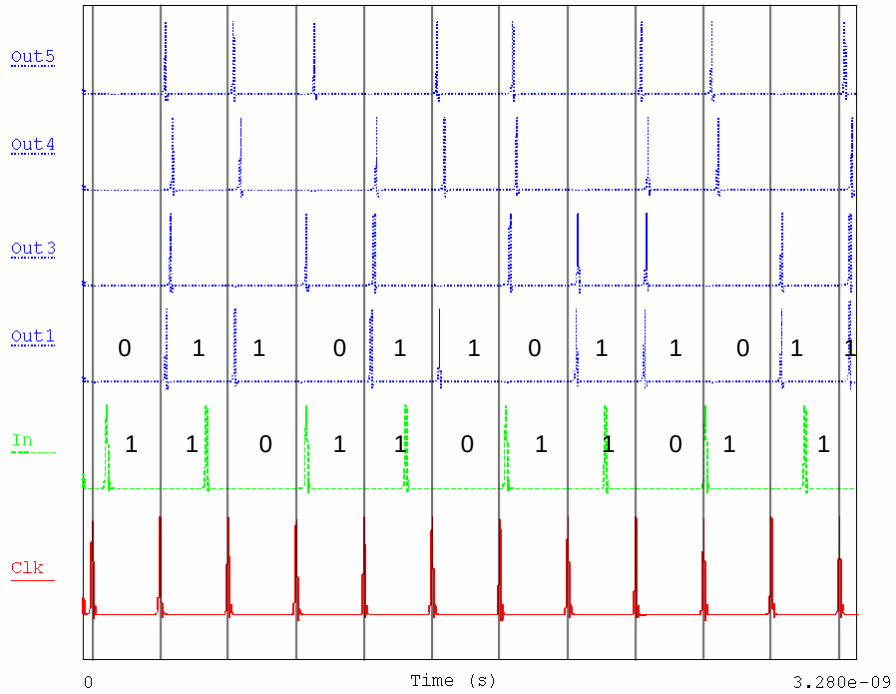

Figure 6.13: Simulation experiments of an RSFQ DFF. Out1 is the fault-free output and Out3 – Out5 are results from defect-induced DFFs showing various fault patterns; Out3: defect3, Out4: defect4, Out5: defect5 from Table 6.3 (y-axis not to scale).

6.6 Simulations of the RSFQ DFF

Knowledge about the behaviour of a defective circuit is essential in finding the effectiveness of the proposed fault models. Simulations were carried out with respect to the HYPRES DFF to predict the behaviour as well as observing faulty behaviour of the outputs arising from the probable defects. Extensive fault simulations were carried out for all 32 defects. However, in future, while investigating possible ATPG approaches, current-based simulation is worthwhile to be carried out after the verification of the fault models. This is due to the fact that the present fault models are not yet verified by voltage-based hardware tests and current-based hardware testing in SCE is still in its infancy.

Part of the results from our approach is presented in Figure 6.13. “Clk” and “In” refer to the clock and input signals and Out1-Out5 (Out2 not shown) show the output signals from “Out” for different cases. The y-axis is rescaled so as to fit all the signals. A typical SFQ pulse has a pulse height of 0.5 mV. The input signal in the test bench of the simulation was “11011011011” and was simulated at a frequency of 3.2 GHz. Out1 shows the fault-free operation of the DFF. The expected output vector is “011011011011” as shown in the figure. Out 3-5 show faulty operation of the DFF revealing clear (faulty) patterns. Out3 is obtained if defect 3 from Table 6.3 was induced in the circuit. The resulting output vector

is “010110111011”. Out4 and Out5 result if the induced defects are defect 4 and 5 in Table 6.3 respectively. Out4 delivers “011011101101” and Out5 “011101101101”.

Table 6.4: Simulation results of the defect-induced HYPRES DFF circuit. Four vectors in the test bench were used (See text for details).

Defect Number	Applied test vector and corresponding results			
	10101010101	**11011011011**	**11101110111**	**10010010010**
1	00000000000x			
2	010101010101	011011011011	011101110111	01001001001x
3	000100100101	010110111011	000101010101	00001001001x
4	101001101001	011011101101	101110111101	10010010001x
5	010101010101	011101101101	101101110111	01010010010x
6	N/A			
7	010101010101	011011011011	0101110111x	01001001001x
8	N/A			
9	00000000101x	00000011011x	000001011101	00000000000x
10	00101010101x	001011011011	001101110111	001001001001
11	010101010101	011011011011	011101110111	01001001001x
12	N/A			
13	010101010101	011011011011	0101110111x	01001001001x
14	010101010101	011011011011	0101110111x	01001001001x
15	10101010101x	11011011011x	110111011101	10010010010x
16	000100100101	00010010101x	000101010101	00001001001x
17	00000000101x	00000011011x	000001011101	00000000000x
18	000000000101	00000001101x	000000101101	00000000000x
19	010101010101	011011011011	011101110111	01001001001x
20	00010101001x	00010101011x	001010101101	00010010010x
21	010101010101	011011011011	011101110111	01001001001x
22	101110011001	11011101110x	111011011101	100110011001
23	000101010101	001011011011	001101110111	00001001001x
24	N/A			
25	00000000000x			
26				
27				
28	010101010101	011011011011	01110111011x	010010010010
29	010101010101	011011011011	011101110111	010010010010
30	00000000000x			
31				
32				

The simulation was repeated by using three different test vectors. The other vectors that were used are “10101010101”, “11101110111” and “10010010010” changing basically the time period for which the DFF will be in its “1” state. The expected correct output vectors are “010101010101”, “011101110111” and “010010010010” respectively. The results from these simulations are summarised in Table 6.4. The first column shows the reference number of the defect in Table 6.3 and Figure 6.12. The next four columns show the result of the simulations on applying the input vectors “10101010101”, “11011011011”, “11101110111” and “10010010010” respectively, denoted by vector 1 to vector 4. The “don’t care” value “x” is applied at the end since the next “clk” signal has not arrived yet and there is still a probability of the logic to become “1” if an output signal arrives before the next “clk” signal (see RSFQ timing protocol described in Chapter 2 of this thesis). The shaded cells in the table represent the undetected faults in the circuit.

It can be seen that certain faults are not susceptible for certain patterns. For e.g. defect 5 in the table is not susceptible to vector 1 while defect 7, 13 and 14 are not susceptible to vector 1 and 2. Six of the defects were undetected by all the test vectors and four of the simulations did not result in any logic value as the circuit simulation had become totally unstable by the induced defect since the bias line was shorted to that particular location denoted by “N/A” in Table 6.4. This oscillation is due to non-convergence of equations in JSIM simulator. This does not always mean that a defect is not detectable in reality.

These results are interesting since identification of the fault by means of the resulting output signal pattern for a given input signal pattern is possible and hence an ATPG approach seems promising in future if CAD tools are used extensively for the involved steps. Even though more information can be derived from these results, our present focus is on verifying the developed fault models, without which the simulation results and derived conclusions becomes theoretical.

6.6.1 Limitations of the Modelling Approach

There are some limitations in the present modelling approach as some of the superconductor phenomena are not able to be translated directly into models. For example, in the case of flux trapping in a JJ, researchers have found that the I_C of the JJ decreases [17]. In the case of an open JJ, the present model is constructed such a way that it works as a reduced-area junction. But in case of flux trapping in the open-region, the experimental results can vary on a case-to-case basis as observed in the case of real RSFQ circuits.

Another drawback is that the present simulator JSIM will not allow a resistance of 0 Ω and near zero values for example in the case of a short between bias and ground. It will generate an error in the simulator. As a result of this, for example the fault simulation for the intra-layer short in M1 (defect 11 in the table) that connects the bias line to the ground indicates a perfect operation of the circuit! But, as mentioned before, this does not mean that this defect is not detectable in reality.

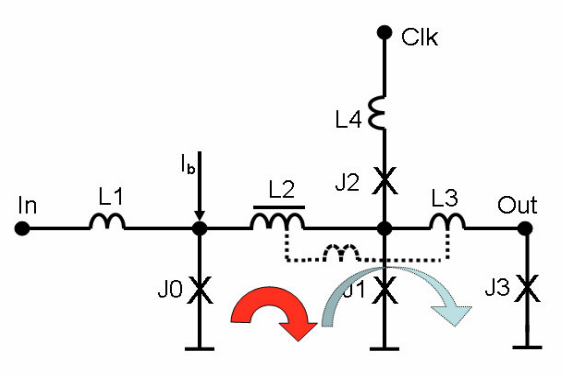

Figure 6.14: Modified DFF schematic showing the formation of a new loop (dotted line) in case of defect2 from Table 6.3 (short between intra-layer M2).

Yet another drawback results from the allowed circuit margins in SCE. As mentioned in Chapter 3 of this thesis, circuits are designed for 60% local and 30% global margins. Due to this, an intra-layer short in M2 from L2 to L3 indeed changes the values of inductances (defect 2), but the output provides correct results. However, there is a probability of trapping a flux in the newly formed "loop structure" (for e.g. see Figure 6.12 and Figure 6.14) which can violate the simulated behaviour. In Figure 6.14, the dotted line shows the new inductor formed due to the intra-layer short from L2 to L3 with a new super-conducting loop (lightly shaded). The junction J3 belongs to the next section of the circuit. This is because the parasitic inductance cannot be incorporated in the model as it violates the input format of the JSIM simulator. Simulation aborts with the following warning "voltage source / inductor loop found including Lx", Lx being the introduced parasitic inductance. Hence, JSIM simulator is found to have limitations which need to be addressed in the future.

Finally, only single faults are assumed in the CUT. Occurrences of multiple defects are probable and require further investigation in detail. Additionally, detailed investigation into delay faults is also required in RSFQ [18], [19]. It is also evident that some of the physical defects will not cause a fault in an SCE circuit. It could be the reason why many complex devices were developed in SCE even without a systematic test methodology. This will make the DBT approach even more challenging. Due to time limitation, these issues have to be addressed in future research.

6.7 A Methodology for the Verification of Fault Models

For the purpose of verification of the proposed fault models, specific defects are induced deliberately by us in the layout at the identified defect-prone areas in the CUT to study the actual behaviour by measurements. The defect-induced circuits are then realised and tested. The simulations were carried out at 3.2 GHz, which is the maximum frequency that can handled by the digital signal generator at the MESA+ Test Centre. The

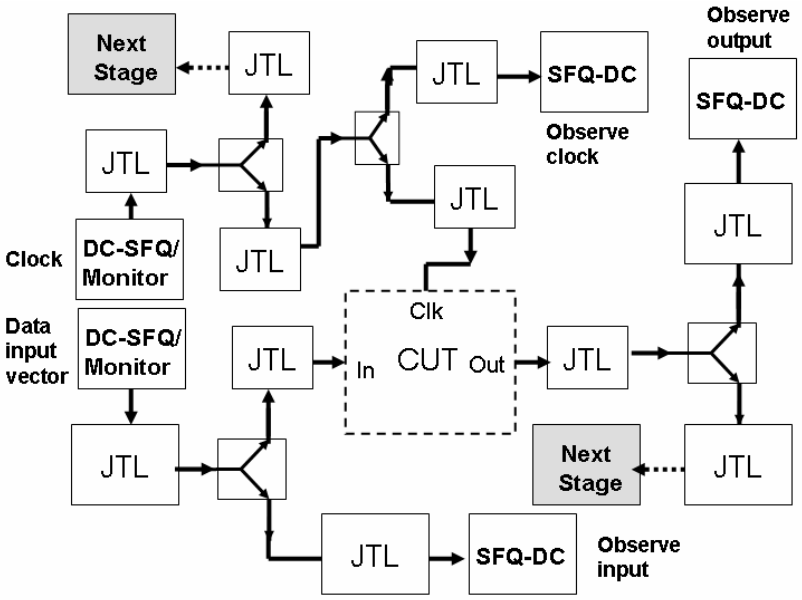

Figure 6.15: DfT scheme for a general multi-stage single-input synchronous RSFQ logic gate. Insertion of paths for monitoring of signals at the CUT nodes has been included.

experimental results have then subsequently to be compared with the simulation outputs to verify the proposed fault models.

6.7.1 Proposed DfT Scheme for Model Verification

A DfT scheme using the proposed observation circuit [20], [21], as described in the third chapter of this thesis, is shown in Figure 6.15. Here, a general schematic is shown for a synchronous multi-stage single-input RSFQ logic gate. The input signals are monitored using an SFQ-to-DC converter at the (external) nodes of the CUT. The "DC-SFQ/Monitor" is an integrated SFQ pulse generator and monitor where the test signals are applied. "JTL" refers to Josephson Transmission Lines. The block with arrows shows the splitter, one of the elements of the SUNY RSFQ cell library [22] mentioned in the previous section of this chapter, which is being used as the observation circuit.

The input signal from a voltage pattern generator is applied to the "DC-SFQ/Monitor" and is transferred to the CUT through a JTL and splitter circuit. The clock signal is also applied in a similar way. To reduce the complexity of the verification circuit, this scheme was simplified for the actual implementation of fault model verification. In this way, the probability of faults in the support structures as well as complication in the debugging of faults has been reduced. The simplified scheme is shown in Figure 6.16. The shaded parts show the external test equipment being used for the verification experiments. The digital signal is converted to an SFQ pulse by a DC-to-SFQ converter and is applied to the input "In" of the DFF via a JTL and splitter circuit. One of the outputs of the splitter is connected to an SFQ-DC converter for monitoring the status of the pulse before entering the CUT.

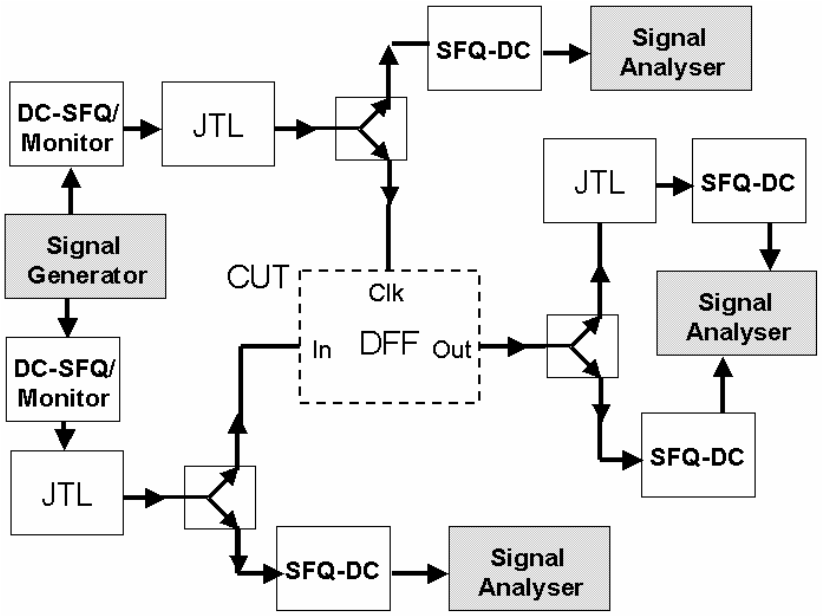

Figure 6.16: Schematic of the test circuit used for the verification of fault models in which the CUT is a defect-induced DFF. The shaded portions indicate external test equipment at room temperature and the non-shaded part is the test chip at 4 K.

The output of the SFQ-DC converter can be observed using a conventional oscilloscope, as the voltage level will be around 800 mV. Similarly, the clock pulse "Clk" is also monitored. The output "Out" is monitored twice, one passing through a similar JTL and the other direct from the splitter. This helps in detecting the delay of the JTL circuit. A defect in the splitter (for e.g. see Section 6.2) or JTL can be identified by the output of the corresponding monitor. A defect in one of the support structures will make the circuit untestable.

6.7.2 Defect Insertion in the RSFQ DFF

For the verification of fault models, deliberate defects have been inserted into the layout of a DFF as CUT and connected to the measurement scheme as described in the previous sub-section. Insertion of defects into the DFF is achieved by means of layout modification. Only the first 24 defects in the list were inserted due to limitation in the available chip area. In SCE, due to its superconducting nature, the wire width of a given connection influences the currents flowing in accordance with the critical current densities of the wiring layer. As a result of local heating, the defective connection can go into resistive state thereby allowing only a small fraction of the currents to flow through the defective path. This resistive behaviour has been observed while at HYPRES in via contacts in SCE. This can cause a defective circuit to perform well in practice. Contrarily, a lithographic limitation will not allow connections of widths smaller than certain dimensions. Hence, care should

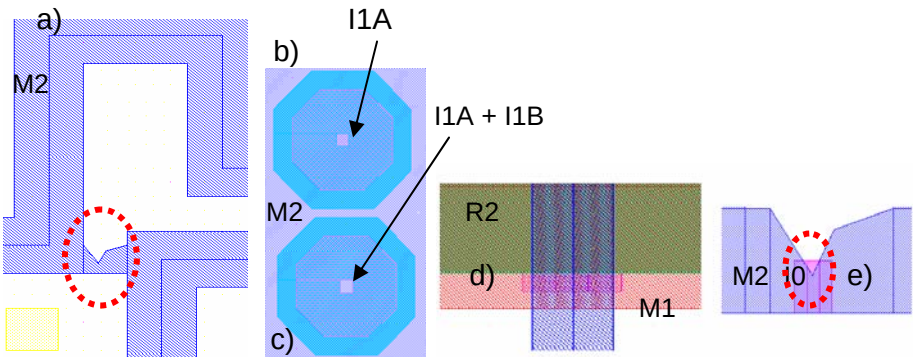

Figure 6.17: Details of induced defects, parts of the DFF are shown - a) a short in M2; b) a short in a JJ – removal of the layer I1A; c) an open JJ - removal of both the layers I1A and I1B; d) M2- R2 short and e) crack in M2.

be taken while inserting a defect into circuits. Also, if the modified (defective) connection is large, for example if it is of the size of the wiring dimensions of the layer, this will not represent a realistic defect. This is due to the fact that most often the defects in reality are for e.g. micro-bridges [23] as presented in Chapter 4 of this thesis.

The following assumptions were made to insert defects. The wire width was reduced for an intra-layer short to 25% of the minimum wiring dimension specified by design rules [24] as the point of short. This will produce a fairly realistic short in the wiring layer while processing. Much more critical is the insertion of an inter-layer short. A via will be formed in case of an excessive short which is a very unrealistic connection in the case of a defective short. This has been tackled by removing the isolation only at the edge of one of the layers in which the short is to be present. The processed chips have to be analysed by scanning- electron microscope or transmission-electron microscope (SEM/TEM), to verify the induced defects. Some examples will be presented in the following sections.

Figure 6.17 shows the details of some of the inserted defects. An intra-layer short is the simplest to implement by an additional metal layer as placed in Figure 6.17a. In this case, defect 2 in Table 6.3 is created as explained in the earlier paragraph.

Shorts and opens in a JJ are inserted as mentioned in chapter 4 of this thesis. For a short in a JJ, the I1A layer that defines the tri-layer was removed as shown in Figure 6.17b. For opens, both I1A and I1B were removed from the layout as shown in Figure 6.17c.

For inter-layer shorts, the concerned isolation layer is removed at the edge of the overlapping position of the two layers. Figure 6.17d shows an example of an inter-layer short between M2 and R2.

An intra-layer short and open can also be introduced by a Focus Ion Beam (FIB) if contamination is avoided carefully, but was avoided as it was decided to carry out one

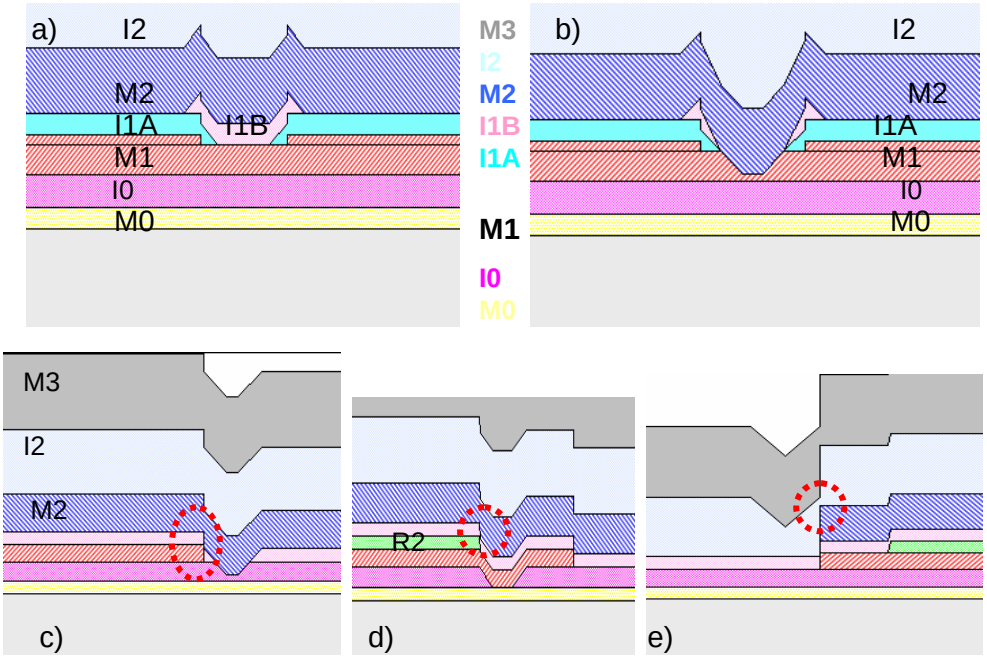

Figure 6.18: Cross-sections of induced defects - a) an open JJ; b) a shorted JJ; c) M2-M1 short; d) M2-R2 short; e) M3-M2 short. In the case of M3-M2, the cross-section does not show an actual short, but is expected to occur in processing due to its extreme proximity [24].

method due to lack of time. This would be the option for these two defects in case the layout modification method fails to provide proper results.

A crack is emulated by considerably reducing the wire width at the concerned position to about 30% of its original value and removing the isolation layer underneath to create a step near the area of minimum contact. Figure 6.17e shows the emulation of a crack in M2. The cross-sections of the inter-layer defects are shown in Figure 6.18 for a better understanding of the defect insertion. Figure 6.18a and Figure 6.18b show an open and shorted JJ in the layout. M2-M1 short, M2-R2 short and M2-M3 shorts are shown in Figures 6.18c-e respectively. Since CADENCE does not allow cross-sectional views, they were made using L-edit from Tanner EDA [25] after adapting it by us to be used with HYPRES Nb technology.

Table 6.5: Details of defect insertion by layout modification

No.	Defect Type	Defect Insertion Realisation
1	M1 short	Additional metal layer M1
2	M2 short	Additional metal layer M2
3	M2 crack/open	Decrease wire width of M2 and removal of isolation layer I0 under the decreased area of M2
4	M2 - M1 bridge	Removal of I1B at the M1 edge with M2
5	M2 - R2 bridge	Removal of I0 at the R2 edge with M2
6	M3 - M2 bridge	Removal of I2 at the M2 edge with M3
7	Tri-layer short	Removal of I1A layer over a JJ
8	Tri-layer open	Removal of I1A and I1B layers over a JJ

The details of insertion of the defects in the layout are given in Table 6.5. The second column shows the type of the defect and the third column specifies how the insertion is being implemented in the layout. Test circuits were designed with fault-free and faulty devices. The first twenty-four defects from Table 6.3 were inserted into the test circuits. Three defects, one of each type: a short, an open and a bridge, were placed twice as back-up. These 27 defects fall into one of the mentioned defect types indicated in the second column of Table 6.5. Three test-chips have been designed incorporating 33 circuits of which 27 are defective as mentioned above. The layout of one of the chips is shown in Figure 6.19 and a photomicrograph in Figure 6.20. Chip dimensions are 5.15 x 5.15 mm^2. The test-access pads have to be wire-bonded to the cryo-probe before the experiments.

Figure 6.21 shows some example micrographs of the induced defects in the DFF. Figure 6.21a shows an actual intra-layer short in the M1 layer (defect 4 from Table 6.3). Figure 6.21b shows the emulation of a crack/open in the layer M2 (defect 1 from Table 6.3) and Figure 6.21c shows an intra-layer short in the M2 layer (defect 2 from Table 6.3) along with a second short due to a random defect shown in the dotted circle.

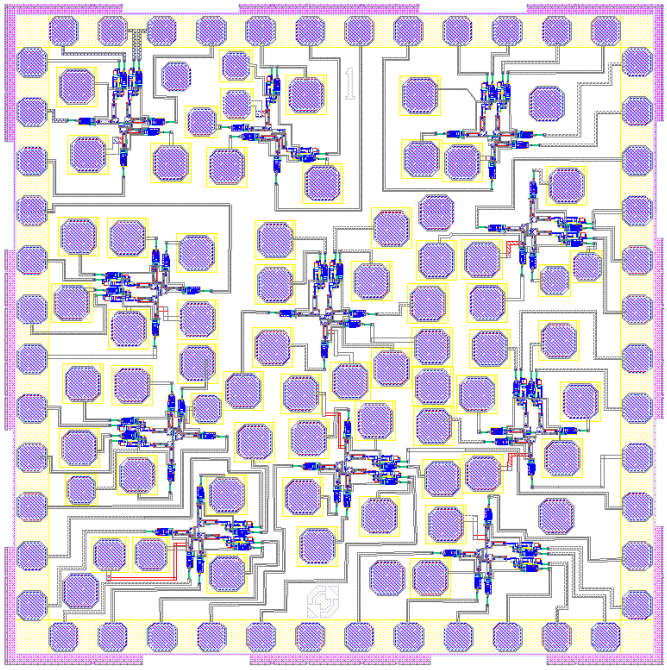

Figure 6.19: Layout of one of the developed test-chips for the verification of fault-models.

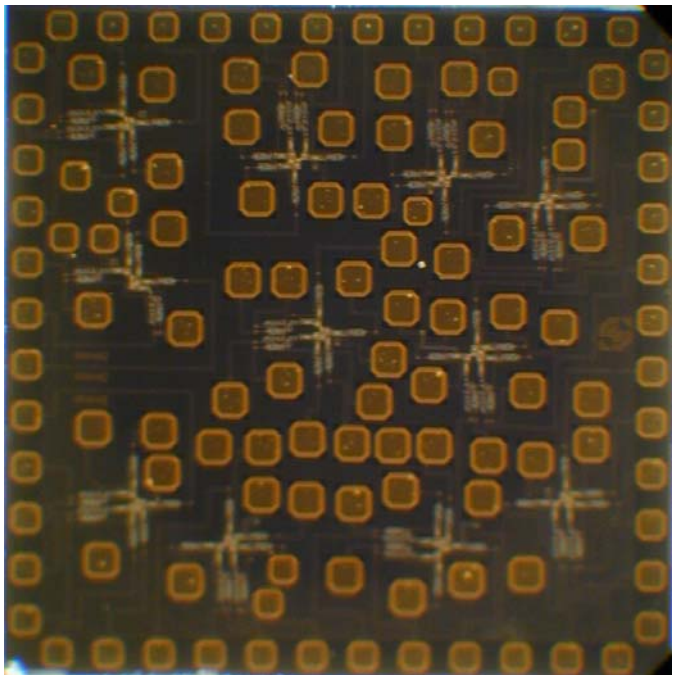

Figure 6.20: Photograph of the previous developed test-chip for the verification of fault-models.

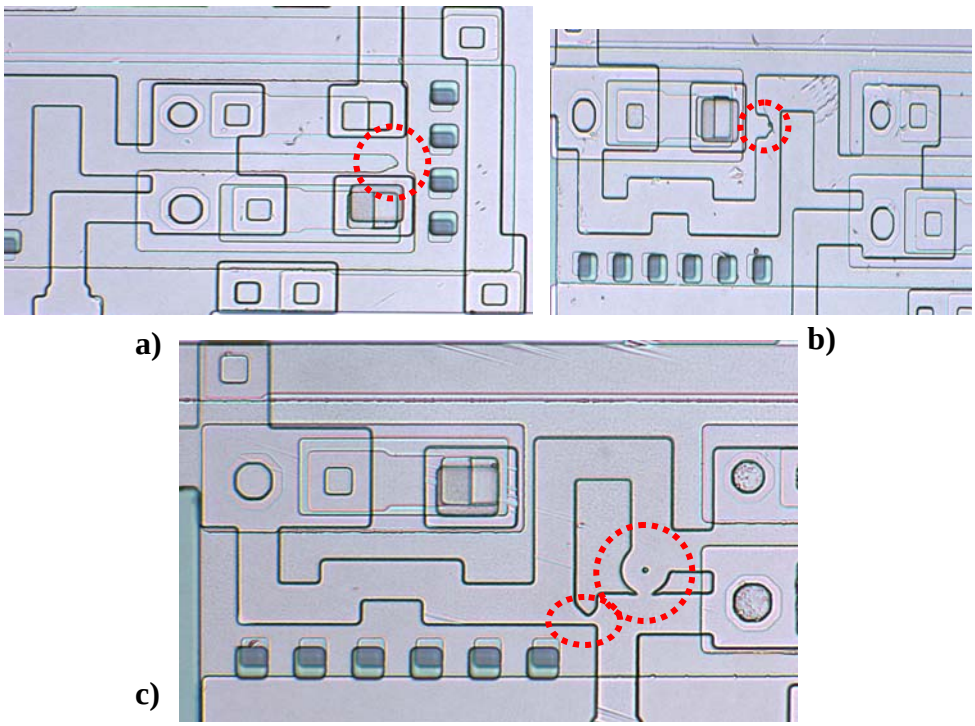

Figure 6.21: Photomicrographs of induced defects. a) short in the layer M1, b) emulation of a crack in the M2 layer and c) an induced short (oval) along with a random process defect causing a second short (circle).

6.7.3 Limitations of the Methodology

Since time-consuming circuit development was avoided by using a readily available cell library for the HYPRES process, available features were limited and had to be adapted to the cells that were available. This mainly limits the observable nodes in the CUT. Also, the occurrence of a random defect in the support cells could make the CUT non-operable. Although this situation can not be avoided, the monitors can detect the presence of defects in the supporting cells. The designed test chips are populated with circuits which could increase the number of defects compared to a normal situation (eleven versus two or three). There is a higher probability of flux trapping due to this high-density. These practical problems can be overcome by careful experiments. Furthermore, the insertion of defects was a challenging task. All locations in the test-chips have to be analysed by SEM/TEM to make sure that the expected defect has occurred in reality and other defects are not present in the circuit. If a defect has not occurred in processing, for example in the case of an M3-

M2 short (e), the I2 layer has to be removed including the M2 layer by shifting the current position of the I2 slit. This requires another design and processing stage.

6.8 Implementation of a Test Scheme for Verification

The experimental setup for the verification of the fault models is shown in Figure 6.22. A Dewar, which contains boiling liquid Helium (He), keeps the chip at 4.2 K. The chip is wire bonded to the cryo-probe using a PCB and mounted in the He Dewar. The cryo-probe head is fitted with connectors for the external equipment. An SCE circuit is very sensitive to RF and magnetic fields and can cause stray flux-tapping in the JJs [26]. Hence, the cryo-probe is fitted with a magnetic shield and is enclosed in an RF-shield. The measurements have to be carried out at the BCT due to the reasons mentioned in chapter 5 of this thesis. A DC power source is used to avoid AC noise in the circuit. An LNA can be connected to the probe-head if necessary (not used) for the amplification of signals in the milli-volt range from the chip to the test equipment.

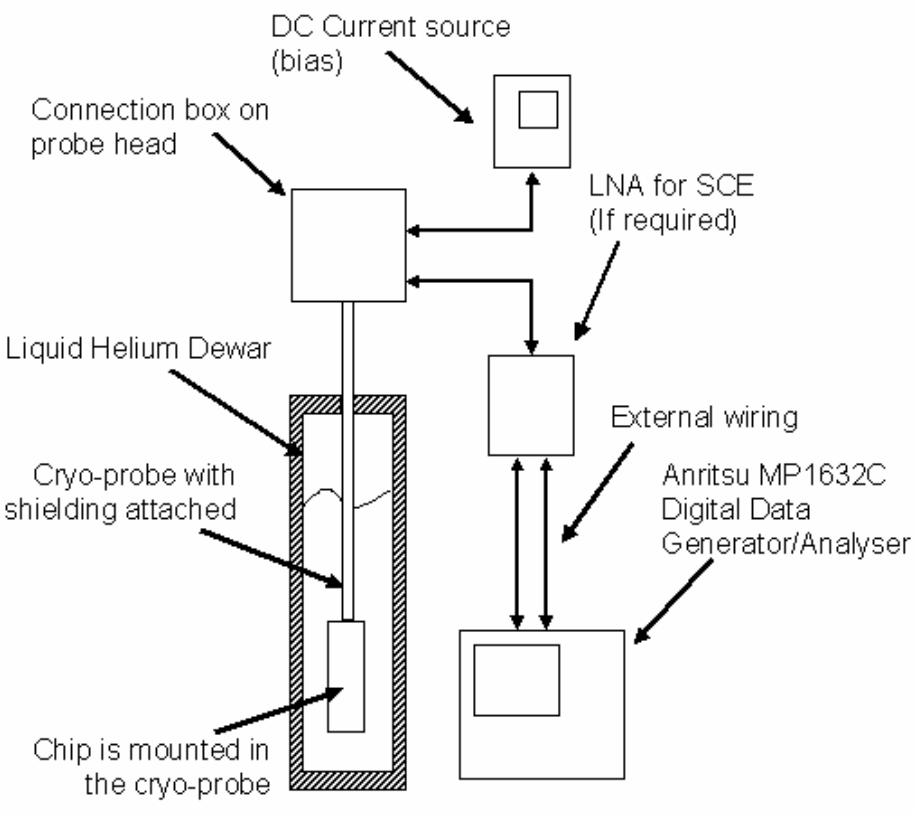

Figure 6.22: Schematic diagram of the experimental set-up for the verification of fault models in SCE.

A special PCB has to be used to deliver the signal from the high-frequency cables to the chip. The high-speed test equipment used for the experimental verification of fault-models is an Anritsu MP1632C digital data generator/analyser [27]. The required data is generated at 3.2 GHz. Bit Error Rate (BER) measurements [28] can also be carried out using the error-detector module in the MP1632.

Due to the up gradation of fabrication facilities at HYPRES, the realisation of the design was delayed by seven months. Finally, on receiving the chips it was found that a scaling error had occurred which had been unnoticed. Furthermore, the delivered chips were out of specification making the chip unusable and the time span required for a re-processing was beyond the scope of this thesis. Due to the above reasons, experimental verification of the chips was not carried out. This will be remaining as important part of future research.

6.9 Conclusion

This chapter presents the latest results in defect-based testing for RSFQ circuits. Detailed fault models for RSFQ circuits have been presented. Extensive simulation experiments on a D-type Flip-Flop using the proposed models have been performed. Simulated I_{DDT} testing was carried out for the first time in SCE. A comparison of the simulation results was carried out with respect to voltage-based structural testing. At this stage, no additional benefits were found with current testing as in semiconductors; in fact fewer defects were detected using I_{DDT} testing. But a more detailed study is required before making general conclusions.

An extensive study was carried out on a HYPRES DFF applying the results from the investigation on the fabrication process. 32 probable defect-prone locations were identified for this DFF and extensive simulation experiments were carried out using the developed fault models. The observation scheme was presented in Chapter 3 of this thesis was then proposed to verify the simulation results for establishing verified fault models in RSFQ. Defects were inserted deliberately into the identified locations by layout modification. Three test chips were designed using this approach and an experimental set-up was also prepared for this purpose. A measurement methodology for the verification of the proposed fault models was also presented in detail. The designed test chips have been implemented applying the proposed test approaches for model verification. The presented approach shows that ATPG could be possible for SCE in the future. This will be the next stage of research.

Results from these test-chips will give valuable information about the behaviour of defects in real SCE circuits under 4 K conditions. If proved correct, these fault models will be used for future ATPG in SCE. In case of variation, the models will have to be adapted to incorporate the superconductor effects mentioned in section 6.6.1 on limitations of the approach.

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Chapter 7

Conclusions

This chapter provides the summary of this thesis and a concluding discussion of the results obtained from this research work. Original contributions of the work and recommendations for future research are also presented.

7.1 Summary of the Thesis and Conclusions

A Defect-Based Test (DBT) methodology for Superconductor Electronics (SCE) is presented in this thesis, so that commercial production and efficient testing of systems can be implemented in this technology in the future.

In the first chapter, the features and prospects for SCE have been presented. The motivation for this research and the outline of the thesis were also described in Chapter 1. It has been shown that high-end applications such as Software-Defined Radio (SDR) and petaflop computers which are extremely difficult to implement in top-of-the-art semiconductor technologies can be realised using SCE. But, a systematic structural test methodology had yet to be developed for SCE and has been addressed in this thesis.

A detailed introduction to Rapid Single-Flux Quantum (RSFQ) circuits was presented in Chapter 2. A Josephson Junction (JJ) was described with associated theory behind its operation. The JJ model used in the simulator used in this research work was also presented. RSFQ logic with logic protocols as well as the design and implementation of an example D-type flip-flop (DFF) was also introduced. Finally, advantages and disadvantages of RSFQ circuits have been discussed with focus on the latest developments in the field.

Various techniques for testing RSFQ circuits were discussed in Chapter 3. A Process Defect Monitor (PDM) approach was presented for fabrication process analysis. The presented defect-monitor structures were used to gather measurement data, to find the probability of the occurrence of defects in the process which forms the first step for Inductive Fault Analysis (IFA).

Results from measurements on these structures were used to create a database for defects. This information can be used as input for performing IFA. “Defect-sprinkling” over a fault-free circuit can be carried out according to the measured defect densities over various layers. After layout extraction and extensive fault simulation, the resulting information will indicate realistic faults.

In addition, possible Design-for-Testability (DfT) schemes for monitoring Single-Flux Quantum (SFQ) pulses within an RSFQ circuit has also been discussed in Chapter 3. The requirement for a DfT scheme is inevitable for RSFQ circuits because of their very high frequency of operation and very low operating temperature. It was demonstrated how SFQ pulses can be monitored at an internal node of an SCE circuit, introducing observability using Test-Point Insertion (TPI). Various techniques were discussed for the introduction of DfT and to avoid the delay introduced by the DfT structure if it is required. The available features in the proposed design for customising the detector make it attractive for a detailed DBT of RSFQ circuits. The control of internal nodes has also been illustrated using TPI. The test structures that were designed and implemented to determine the occurrence of defects in the processes can also be used to locate the position for the insertion of the above mentioned DfT structures.

In Chapter 4, detailed investigations with regard to two Low Temperature Superconductor (LTS) RSFQ processes (JeSEF and HYPRES) have been presented. Both processes were described for better understanding of potential defects. The design rules, layouts and real chips were investigated to identify potential weak spots in the processes. The investigations resulted in a list of probable defect locations in the processes. Associated test structures were developed as part of this investigation. These test structures are capable of detecting and localising the relevant defects.

The first process that was investigated is an academic process, the JeSEF Niobium (Nb) process from Jena, Germany. A list of 27 probable defects was identified in this process. Since the process was under development, eight test structures, including the ones capable of detecting the four types of defects which were suspected to be the most probable ones were the main focus while investigating this process. Test structures have also been developed for the JJs to be measured at low temperatures. These test structures were incorporated into a test chip, the JeSEF_Jan02 design. Ten identical test chips were placed per wafer on a 6” wafer containing 32-chips.

The second process that was under investigation is the HYPRES Nb process from New York, USA. This is a matured commercial process compared to the JeSEF process. In this case, a list of 31 probable defects was identified. A much detailed analysis has been carried out on the HYPRES process since more circuits (cell libraries) were developed and available in this process. Detection of defects in all possible interconnects were the primary concern as the HYPRES process was a more mature process in which parametric variations were stated to be of less concern. Thirty-eight test structures were developed for the Room Temperature (RT) measurements. Nineteen different structures were designed for Low Temperature (LT) measurements including the defect-induced JJs. Three identical test chips (design HYPRES_Nov03) were placed per wafer on a 6” wafer containing 200+ chips.

The number of predicted defects does not reflect any information about the quality of the process, but are predicted according to the topography of the process. These defects have been grouped into a list of probable defect locations for the classification of defects in an RSFQ process. The defects in a JJ are related to its thin dielectric-barrier. Shorts, opens and pinholes can cause junctions to malfunction. Opens and near opens in metal layers form another class of defects, resulting from the step-coverage profile of the underlying layers. Via-contact defects due to isolation problems and resistor-layer problems are other probable defect classes.

Measurement results from the designed structural test chips have been presented in Chapter 5. A quantitative data analysis has been performed with regard to the room temperature structures while a qualitative approach on low temperature structures showed that the proposed approach is suitable for a quantitative analysis in the future.

Since ten chips per wafer were available from the JeSEF process, a detailed wafer mapping could be performed. Since it was a less mature process, less number of different defect-monitor structures were implemented compared to the HYPRES process. The

measurement data from the developed test structures proved that they are capable of extracting defect information for SCE circuits being processed at JeSEF.

The HYPRES process was extensively analysed by implementing different types of defect-monitor structures. Only three chips were available per wafer in the HYPRES process. Hence the results were limited. In addition, the foundry upgrade and renovations at HYPRES have negatively affected the statistics by increasing the probable defects. A ranking list was prepared from the 25 different defects.

From both processes it was concluded that the step-coverage at the via interconnects pose a significant problem. This information will be useful for inductive fault analysis while developing an Automatic Test Pattern Generation (ATPG) approach for RSFQ circuits.

Chapter 6 presents the latest results in DBT for RSFQ circuits. Detailed fault models for RSFQ circuits have been presented. Extensive simulation experiments on a DFF using the proposed models have been manually performed using DBT techniques. I_{DDT} testing simulation was carried out for the first time in SCE. A comparison of the simulation results was carried out with respect to logic-based structural testing. At this (initial) stage, no additional benefits were found with current testing as in semiconductors; in fact fewer defects were detected using current testing. But a more detailed study is required before making general conclusions.

A measurement methodology for the verification of the proposed fault models was also presented. Three test-chips have been designed and implemented applying the proposed measurement approaches for model verification. Results from these test-chips will give valuable information about the behaviour of defects in real SCE circuits under 4 K conditions.

7.2 Original Contributions of this Work

The following are the original contributions of this work:

A detailed study into comparative RSFQ process defects was carried out for the first time and has helped foundries to improve the quality of their proccess.

An academic and a commercial process were investigated as part of the conducted research. Defect-monitor structures were developed for those processes based on design rules, circuit designs and anticipated defects. Realisation of test chips for the processes and data on realistic defects were provided. The results from this thesis prove that the developed structures are capable of detecting the probable defects.

A DfT technique to be used in the verification of fault models was demonstrated for RSFQ circuits. Fault models were proposed for RSFQ circuits from the study on process defects. A DBT methodology was applied to RSFQ circuits for the first time. Possibilities for Test Pattern Generation (TPG) for RSFQ circuits were investigated by a limited manual

insertion of defects and extensive simulation experiments. The feasibility of an I_{DDT} testing was investigated for the first time in SCE by means of simulation.

A Built-In-Self-Test (BIST) architecture for SCE ADCs was suggested for the first time and verified in VHDL. It was also proved that the required hardware for the BIST can be implemented in SCE.

Test chips were developed to verify the proposed fault models. This kind of work was carried out for the first time in SCE. Test schemes were proposed for the purpose of verification of these models. Realisation of the test chips was carried out but due to errors mentioned in Chapter 6 of this thesis, measurements could not be carried out.

7.3 Recommendations for Future Work

Since the low-temperature measurement has proven to be extremely time consuming, the original idea to do all measurements at room temperature is very relevant. Currently, only an indication that the proposed approach is good for the detection of defects is available from the presented experiments. An efficient system has to be developed and the defect behaviour has to be translated to room temperature values to provide useful statistics using quantitative data. This is the next step that has to be carried out in the future.

Fault models have to be verified using the DBT methodology presented in Chapter 6. The experiments on the logic test chips for the verification of fault models have to be carried out. The verification experiments could not be carried out due to the delays and fab upgrades. So a reprocessing of the test chip has to be carried out using an updated cell-library. If verified, these fault models should be used for IFA (time-consuming) and fault simulation to generate structural test vectors. Detailed research into automation of the TPG for SCE is also an important step in the future. If proved correct, these fault models will be used for future ATPG in SCE. In case of deviation, the models will have to be adapted to incorporate the superconductor effects mentioned in Section 6.6.1 on limitations of the approach.

Statistics on LT structures (very time consuming) is not yet available as only qualitative results were obtained. An efficient probe has to be developed for this purpose which will reduce the test time and preferably eliminating the wire-bonding process. The LT measurement of RT structures to get a correlation of the behaviour of defects at both temperatures have to be carried out. This is also a very time-consuming process.

Since HYPRES has upgraded the process after the investigation presented in this thesis as mentioned in Chapter 5, a new investigation is required to find the latest top-ranking defects in the process. Extraction of critical area of the circuits and determination of yield in the processes can be carried out for yield-analysis purposes. Information about yield in the investigated processes can also be derived from the results by applying these values to a suitable yield model. Information on how yield is influenced by random defects can also be inferred from this information. Then adequate measures can be taken, depending on the nature of defect, so as to increase the yield.

It was proved by simulations that BIST is possible for an SCE ADC to be used for SDR application and the required hardware can be made in LTS technology. But, further work on testability of an SCE ADC was suspended due to lack of basic information on process defects. This has to be completed to facilitate the commercial production of an SCE ADC.

7.4 Concluding Remarks

SCE finds its application when ultra-high speed switching or processing of large volume of data per unit time is required. This thesis presented a DBT approach for LTS RSFQ circuits. RSFQ process analysis was presented in detail with two case studies. Knowledge about the types of defects that can occur in the process is available after the conducted study. More detailed quantitave measurements have to be carried out at LT for statistics as well as establishing fault-models in SCE. Much work is remaining regarding testing of SCE and this thesis gives a glimpse of a whole new world ahead in testing!

Abbreviations

ATE	Automatic Test Equipment
ATPG	Automatic Test Pattern Generation
BS	Base Station
BER	Bit Error Rate
BIST	Built-In-Self-Test
CUT	Circuit-Under-Test
DBT	Defect-Based testing
DFF	D-type Flip-Flop
DfT	Design-for-Test
EMI	Electromagnetic Interference
FIB	Focus Ion Beam
HTS	High-Temperature Superconductor
HTMT	Hybrid Technology MultiThreaded architecture
ICMS	Integrated Circuit Measurement System
IFA	Inductive Fault Analysis
ITRS	International Technology Roadmap for Semiconductors
JeSEF	Jena Superconductor Electronics Foundry
JJ	Josephson Junction
JTL	Josephson transmission lines
LT	Low Temperature
LTS	Low-Temperature Superconductor
MIPS	Million Instructions Per Second
PCM	Process Control Monitors
PDM	Process Defect Monitors
RSFQ	Rapid Single-Flux Quantum
SCE	SuperConductor Electronics
SDR	Software-Defined Radio
SDR BS	Software-Defined Radio Base Station
SEM	Scanning Electron Microscopy
SFQ	Single Flux Quantum
SIS	Superconductor-Insulator-Superconductor
SINIS	Superconductor-Insulator-Normal metal-Insulator- Superconductor
SNS	Superconductor-Normal metal-Superconductor
SQUID	Superconducting QUantum Interference Device
TEM	Transmission Electron Microscopy
TPI	Test Point Insertion

List of Publications

Journals:

1. A. A. Joseph, M. H. H. Weusthof, and H. G. Kerkhoff, "Application of DfT techniques to a 20 GHz superconductor delta ADC", Microelectronics Journal, Vol. 33 October 2002, pp. 791-798.

2. A. A. Joseph, S. Heuvelmans, G. J. Gerritsma, and H. G. Kerkhoff, "The Detection of Defects in a Niobium Tri-layer Process", IEEE Trans. Appl. Super.cond, Vol. 13, June 2003, pp. 95-98.

3. A. A. Joseph, S. Heuvelmans, G. J. Gerritsma, and H. G. Kerkhoff, "Test Structures and their Application in Structural Testing of Digital RSFQ Circuits", Physica C, Vol. 403, March 2004, pp. 103-11.

4. A. A. Joseph, and HG Kerkhoff "Design for Testability of Superconductor Electronics" Supercond. Sci. and Tech., Vol. 16, December 2003, pp. 1559-1565.

5. A. A. Joseph, J. Sese, J. Flokstra, and H.G. Kerkhoff, "Structural Testing of HYPRES Niobium Process", IEEE Trans. Appl. Super.cond., Vol. 15, June 2005, pp. 106-109.

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1. A. A. Joseph, M. H. H. Weusthof, and H. G. Kerkhoff, “DfT for a Superconducting Delta ADC for Software-Defined Radio Applications”, Proc. IEEE International Mixed-Signal Testing Workshop (IMSTW) 2001, pp. 47-54.

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11. A. A. Joseph and H.G. Kerkhoff, “Testing Superconductor Logic Integrated Circuits”, Digest of papers of the IEEE European Test Symposia Tallinn, Estonia 2005, pp. 239-244.

(Extended) Abstracts:

1. A. Joseph, S. Heuvelmans, G.J. Gerritsma and H.G. Kerkhoff, "The Detection of Defects in a Niobium Tri-layer Process", Proceeding of the IEEE Appl. Super.cond conference, Aug 2002, pp. 8-9.

2. A. A. Joseph and H.G. Kerkhoff "Design for Testability of Superconductor Electronics" Extended Abstracts of International Superconductive Electronics Conference (ISEC 2003), July 2003, pp. PMo071-2.

3. A. A. Joseph, J. Sese, J. Flokstra and H. G. Kerkhoff "Structural Testing of HYPRES Niobium Process", Applied Superconductivity Conference, 2004, pp. 37.

4. A. A. Joseph and H.G. Kerkhoff, "Fault Modeling in RSFQ Circuits for Defect-Based Testing of LTS Devices", Applied Superconductivity Conference, 2004, pp. 76.

5. A. A. Joseph, J. Flokstra and H. G. Kerkhoff, “Structural Testing of RSFQ Circuits”, Extended Abstracts of International Superconductive Electronics Conference (ISEC 2005), pp. PB.13.

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A majority of the readers tend to skip a thesis after introduction and conclusions while most often a greater attention is given to this epilogue a.k.a. the acknowledgement section. So I would like to tell the story in a pleasant manner here. I will be brief else it would fill in another book, which I will leave as future work! ☺

This thesis is the result of few years of my research work mainly carried out in the Netherlands. But, the whole adventure started in early 2000 from a discussion with a fellow student in my hostel room at the Indian Institute of Technology, Madras. I decided to apply, after coming to know about the MESA+ Institute with a potential to make an Electrical Engineering degree, after a Physics Masters, which was a dream right from my Bachelors phase, to work in Microelectronics. And interestingly, each step I made took me to a greater level than I initially expected bringing substantial growth in the process. In the course of time, my childhood ambition to be a scientist was fulfilled with satisfaction when I was given the opportunity to chair a technical section at the top ranking conference in the field of research (ASC 2004), which is an opportunity only a few Ph.D. students receive.

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Arun Antony Joseph